1 GENERAL DESCRIPTION

The SNC86KC 12MHz 16-bit RISC controller series with embedded multi-channel 24-hardware Voice/MIDI Wave Processing Unit (WPU). In addition to having multi-channel hardware channels, one software high quality voice channel with SONiX HQDPCM algorithm is provided.

Key peripherals include a single high quality 14bit DAC with push-pull amplifier, 32-channel comparator for cap sensing touch, three external interrupts, 8/12 PWMIOs, serial peripheral interface (SPI), one 8-bit timer and two 12-bit timers. The device features provide idle mode for real-time clock (RTC) applications and sleep mode for power savings.

The SNC86KC contains a Low Voltage Detector (LVD) for power management usage. The status of internal or external power can be detected and reported to the management software. There is a Low Voltage Reset (LVR) function provided to keep the whole system from losing data when voltage drops to a low level.

1.1. Features

■ CPU

- **Operating voltage: 2.2V ~ 5.5V**
- **System clock: 12.288MHz**
- System clock source:
  - High clock: 32.768KHz crystal PLL to 12.288MHz and 12.288MHz internal ROSC
  - Low clock: 32.768KHz crystal
- Programmable System Clock: 12MHz, 6MHz, 3MHz
- Provides Idle and Sleep mode to reduce power consumption
- General-Purpose I/O ports:
  - 16 ~ 32 programmable I/Os (by body)
  - High drive/sink current
- Timer/Counter
  - 8-bit TimerA Counter
  - Two 12-bit TimerB & TimerC Counter
  - Timer1 (1ms, 4ms)
  - RTC Timer can be programmable: 62.5ms ~ 64sec
  - WDT Timer
  - One 16-bit TimerD with Capture Timer Function
- 3 External interrupt Sources: INT0, INT1, INT2
- **8 ~ 12 Hardware PWMIOs** (by body) with 256-level brightness control
- IR function provided
- Low Voltage Reset (LVR 2.0V)
- Low Voltage Detector (LVD)
  - 4 levels (2.2V/2.4V/2.8V/3.2V)
- **Embedded regulator for SPI Flash**
- **32-channel comparator** for Cap sensing applications
- Serial Peripheral Interface (SPI)
  - Supports master mode only.
  - Supports Single or Quad mode

■ WPU

- **Single 14-bit software channel with noise filter to play high quality sound***
  - 4-bit HQDPCM
  - 5-bit HQDPCM
- **Maximum 24 independent voice channels with noise filter**
- Single **14-bit DAC with push-pull amplifier** for direct drive speaker
- 24-channel with four playing modes by Wave Processing Unit (WPU):
  - 5-bit ASDPCM
  - 6-bit ASDPCM
  - 8-bit ASDPCM
  - 12-bit ASDPCM
- Event Mark function is supported

*Note. Two channel voice play when both at the same sample rate.

1.2. Applications

- Electronic Piano
- High end toy controller
- General Music synthesizer
- General purpose controller

Table of Contents

2 REVISION HISTORY

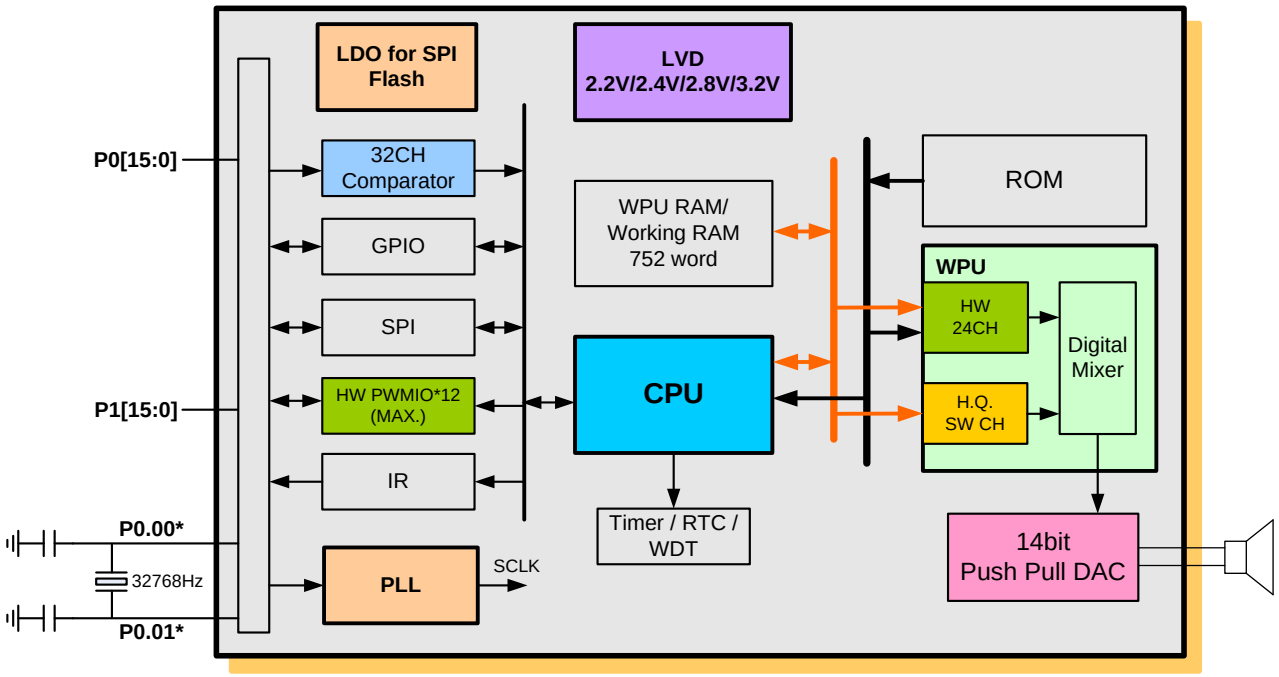
Version	Date	Description
Rev. 1.0	Oct. 03, 2016	First issue
Rev. 1.1	Mar. 03, 2017	1.Add Consumption of Playback in SPI Flash 2.Add Touch Application Current 3.Update ELECTRICAL CHARACTERISTICS
Rev. 1.2	May 03, 2017	Add Package form and Package information
Rev. 1.3	Nov 27, 2017	Add SNC86120C/160C Package form
Rev. 1.4	Apr 19, 2018	Add SNC86060C/080C Package form

3 PRODUCT SELECTION GUIDE

Part No.	Voice Duration	RAM	ROM	I/O	PWMIO	OSC Type	HW Channel	SW HQ Channel	Cap-Touch Key	RTC
SNC86060C	60sec	752*16	96K*16	16	**8**	X'tal / Int. ROSC	24	1*	**0**	Yes
SNC86080C	80sec	752*16	128K*16	16	**8**	X'tal / Int. ROSC	24	1*	**0**	Yes
SNC86120C	120sec	752*16	192K*16	24	12	X'tal / Int. ROSC	24	1*	24	Yes
SNC86160C	160sec	752*16	256K*16	24	12	X'tal / Int. ROSC	24	1*	24	Yes
SNC86200C	200sec	752*16	320K*16	32	12	X'tal / Int. ROSC	24	1*	32	Yes
SNC86240C	240sec	752*16	384K*16	32	12	X'tal / Int. ROSC	24	1*	32	Yes
SNC86280C	280sec	752*16	448K*16	32	12	X'tal / Int. ROSC	24	1*	32	Yes
SNC86320C	320sec	752*16	512K*16	32	12	X'tal / Int. ROSC	24	1*	32	Yes

*Note. The 14bit software HQ channel maximum provides playing two channel voices when sample rate is identical.

4 Functional Block Diagram



*Note. P0.0 & P0.1 is share pin

*Note: (1) Number of Comparator channels by body is 24CH or 32CH or none
(2) Number of PWMIO channels by body is 8 or 12.
(3) Number of GPIOs by body is 16IO or 24IO or 32IO.
(4) PLL/32768 X'tal/RTC function is option by body

5 PIN ASSIGNMENT

SNC86320C/SNC86280C/SNC86240C/SNC86200C bodies

Pad Name	I/O	Function Description
P0.00 ~ P0.15	I/O	Bit0 ~ Bit15 of I/O port 0
P1.00 ~ P1.15	I/O	Bit0 ~ Bit15 of I/O port 1
VDDDA	P	Positive power supply for DAC
GNDDA	P	Negative power supply for DAC
VDDPP	P	Positive power supply for Audio
GNDPP	P	Negative power supply for Audio
VDDSPI	P	Positive power supply for SPI interface
VDD	P	Positive power supply for I/O
GND	P	Negative power supply
REGOUT	P	Positive power supply for Core logic / Regulator output
VDDREG	P	Positive power supply for Regulator circuit
GNDREG	P	Negative power supply for Regulator circuit
RST	I	Chip Reset (Active low)
BN0	O	Direct Drive negative output
BP0	O	Direct Drive positive output
VCOIN	I	PLL Low Pass Filter Input

SNC86160C/SNC86120C bodies

Pad Name	I/O	Function Description
P0.00 ~ P0.15	I/O	Bit0 ~ Bit15 of I/O port 0
P1.00 ~ P1.07	I/O	Bit0 ~ Bit7 of I/O port 1
VDDDA	P	Positive power supply for DAC
GNDDA	P	Negative power supply for DAC
VDDPP	P	Positive power supply for Audio
GNDPP	P	Negative power supply for Audio
VDDSPI	P	Positive power supply for SPI interface
VDD	P	Positive power supply for I/O
GND	P	Negative power supply
REGOUT	P	Positive power supply for Core logic / Regulator output
VDDREG	P	Positive power supply for Regulator circuit
GNDREG	P	Negative power supply for Regulator circuit
RST	I	Chip Reset (Active low)
BN0	O	Direct Drive negative output
BP0	O	Direct Drive positive output
VCOIN	I	PLL Low Pass Filter Input

SNC86080C/SNC86060C bodies

Pad Name	I/O	Function Description
P0.00 ~ P0.15	I/O	Bit0 ~ Bit15 of I/O port 0
VDDDA	P	Positive power supply for DAC
GNDDA	P	Negative power supply for DAC
VDDPP	P	Positive power supply for Audio
GNDPP	P	Negative power supply for Audio
VDDSPI	P	Positive power supply for SPI interface
VDD	P	Positive power supply for I/O
GND	P	Negative power supply
REGOUT	P	Positive power supply for Core logic / Regulator output
VDDREG	P	Positive power supply for Regulator circuit
GNDREG	P	Negative power supply for Regulator circuit
RST	I	Chip Reset (Active low)
BN0	O	Direct Drive negative output
BP0	O	Direct Drive positive output

6 PACKAGE FORM

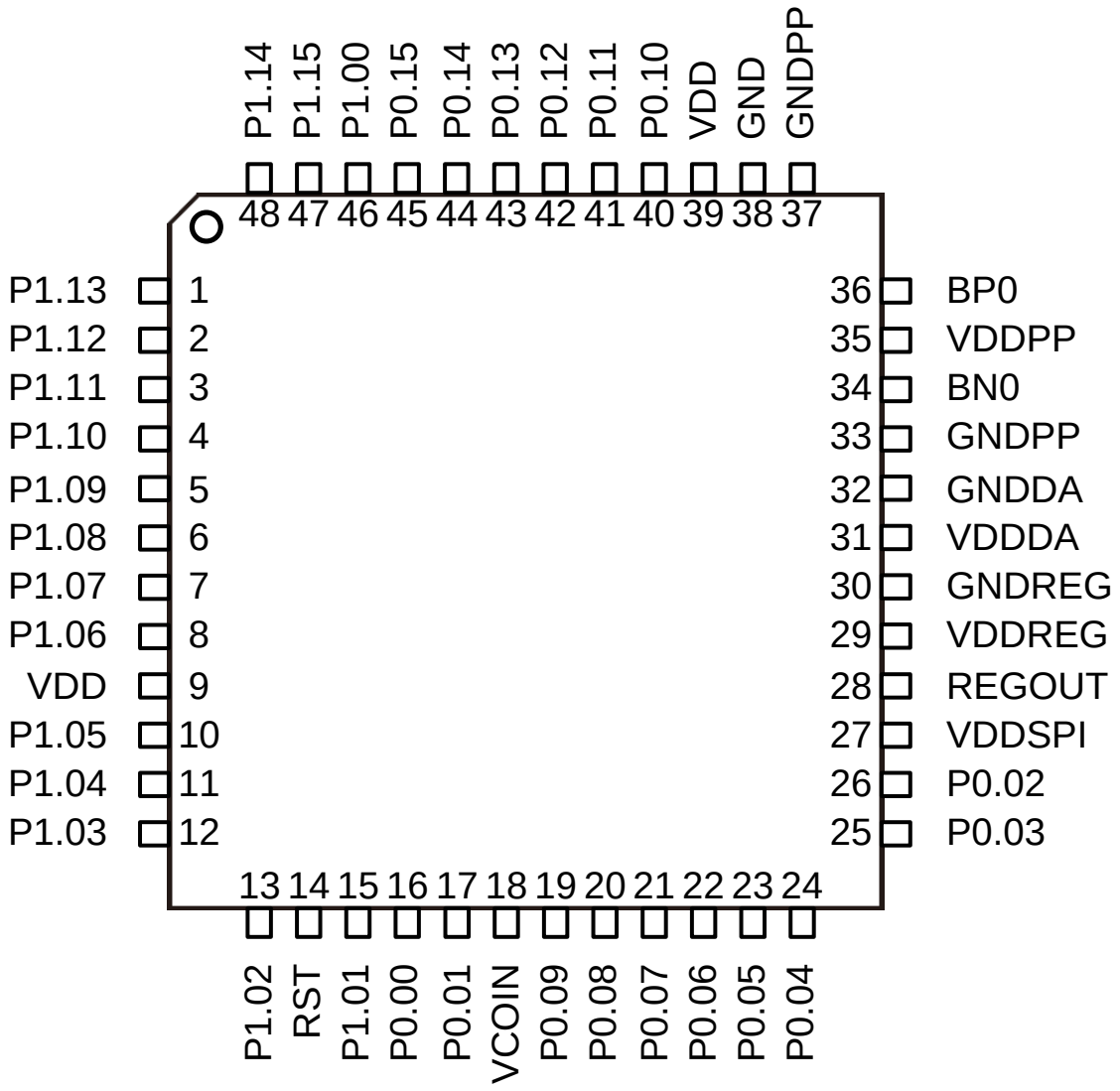
SNC86320C/ SNC86280C/ SNC86240C/SNC86200C

LQFP48

Support 32IO

P0.00~P0.15

P1.00~P1.15



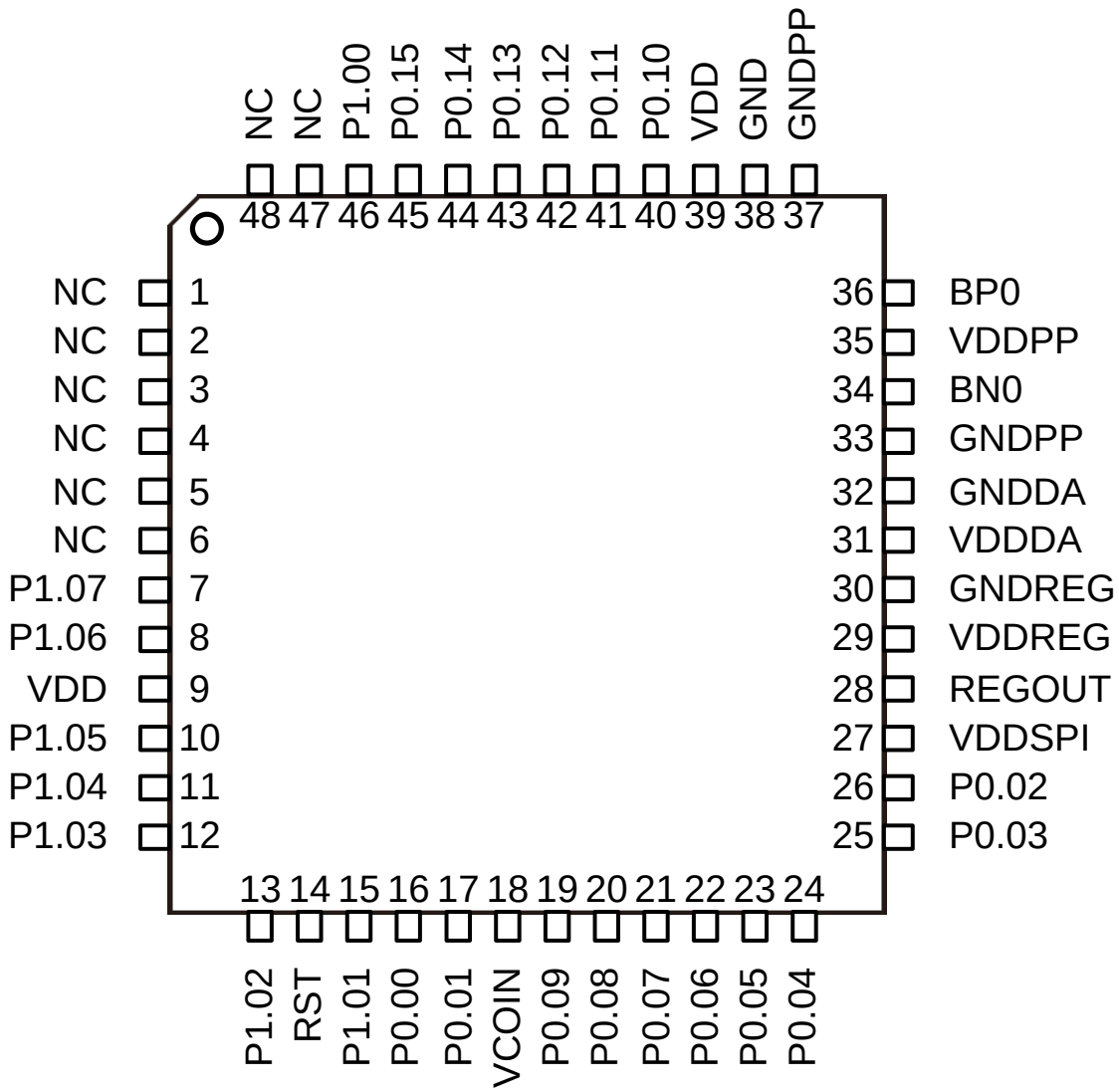
SNC86160C/ SNC86120C

LQFP48

Support 24IO

P0.00~P0.15

P1.00~P1.07

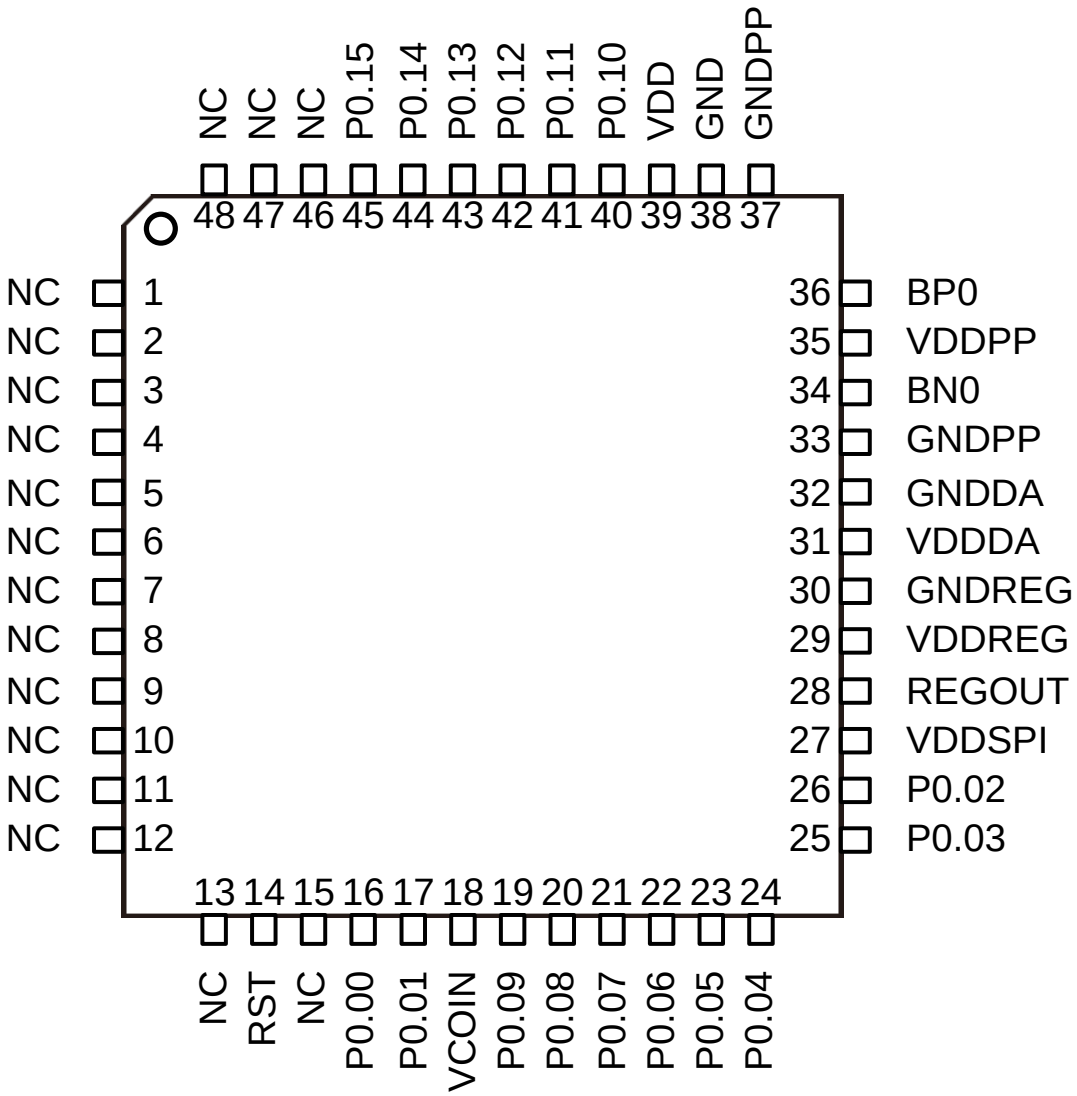


SNC86060C/ SNC86080C

LQFP48

Support 16IO

P0.00~P0.15



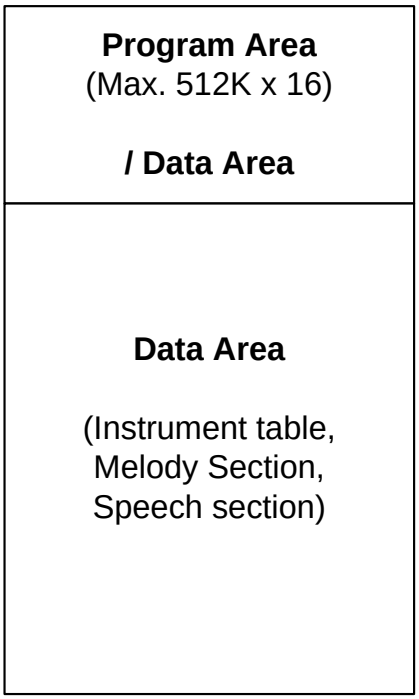
7 FUNCTIONAL DESCRIPTIONS

7.1. CPU Architecture Description

The SNC86KC family CPU is a 16-bit RISC architecture that provides powerful instructions and enhances RAM access to reduce instruction and execution cycles. The CPU is based on 12MHz clock system and contains RAM, ROM, Stack, I/Os, Timer, ALU and interrupt functions.

7.2. ROM

The SNC86KC family contains a substantial amount of internal ROM that is shared by program and resource data. Program data cannot exceed 512K words. The architecture of ROM is shown as follows:



Architecture of ROM

ROM sizes for different bodies is shown in the following table:

Body	ROM Size	Program Address	ROM Address
SNC86060C	96K*16	0x00000 ~ 0x17FFF	0x00000 ~ 0x17FFF
SNC86080C	128K*16	0x00000 ~ 0x1FFFF	0x00000 ~ 0x1FFFF
SNC86120C	192K*16	0x00000 ~ 0x2FFFF	0x00000 ~ 0x2FFFF
SNC86160C	256K*16	0x00000 ~ 0x3FFFF	0x00000 ~ 0x3FFFF
SNC86200C	320K*16	0x00000 ~ 0x4FFFF	0x00000 ~ 0x4FFFF
SNC86240C	384K*16	0x00000 ~ 0x5FFFF	0x00000 ~ 0x5FFFF
SNC86280C	448K*16	0x00000 ~ 0x6FFFF	0x00000 ~ 0x6FFFF
SNC86320C	512K*16	0x00000 ~ 0x7FFFF	0x00000 ~ 0x7FFFF

7.3. RAM

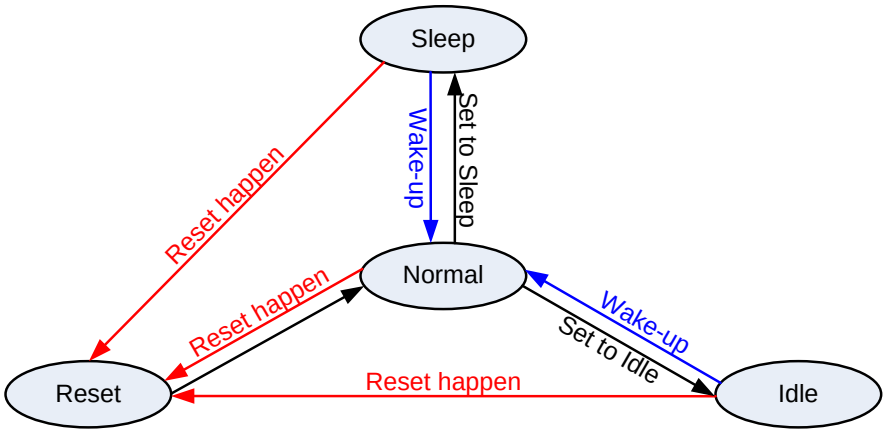
The SNC86KC RAM is separated into several banks. Each RAM bank contains 256 words where the appropriate bank number must be set before access. The RAM is subdivided into 4 banks where each bank contains 256 words. The address table of the RAM banks is shown below.

Bank Num	Address Range	Description	Total Size (word)
0	0x000~0x04F	Special Registers	
	0x050~0x057	Bit Operation for C/User RAM	8
	0x058~0x05D	Reserved for C	6
	0x05E~0x0FF	User RAM	162
1	0x100~0x17F	SW CH/User RAM	128
	0x180~0x1DF	User RAM	96
	0x1E0~0x1FF	Stack buffer	32
2	0x200~0x201	WPU Channel RAM 0/User RAM	2
	0x202~0x203	WPU Channel RAM 1/User RAM	2
	---		42
	0x22E~0x22F	WPU Channel RAM 23/User RAM	2
	0x230~0x23F	User RAM	16
	0x240~0x27F	Un-define	
	0x280~0x287	WPU Channel RAM 0/User RAM	8
	0x288~0x28F	WPU Channel RAM 1/User RAM	8
	---		104
	0x2F8~0x2FF	WPU Channel RAM 15/User RAM	8
3	0x300~0x307	WPU Channel RAM 16/User RAM	8
	---		112
	0x338~0x33F	WPU Channel RAM 23/User RAM	8
	0x340~0x37F	User RAM	64
	0x380~0x3FF	Un-define	

7.4. Operation Modes

The SNC86KC operates in three modes for different clock rates and power saving purposes. There is one active mode as well as two software selectable low-power modes of operation. GPIO or RTC event can wake up the device from any of the two low-power modes.
The following three operating modes are configured by software:

- **Normal Mode：**
  - All clocks are active
  - System clock rate can selectable from 12MHz to 3MHz
- **Idle Mode：**
  - CPU is disabled
  - Only Low-speed clock is turn on
  - RTC Mode
- **Sleep Mode：**
  - CPU is disabled
  - High and Low speed clock is turn off



Operating Mode Control Block

SNC86KC function status in all Operating Modes:

Mode / Device	Sleep	Idle	Normal
IHRC(High CLK)	X	X	O
PLL(High CLK)	X	X	O
ILRC(32768Hz)	X	O	O
X'tal(32768Hz)	X	O	O
CPU	X	X	O
Interrupt	X	X	O
WPU	X	X	O
SPI	X	X	O
PWMIO	X	X	O
IR	X	X	O
Comparator	X	X	O
PPDAC	X	X	O
Timer	X	X	O
RTC	X	O	O
LVD	X	X	O
LVR	O	O	O

Note: In normal mode, software is used to change operation to sleep, idle, or normal modes.

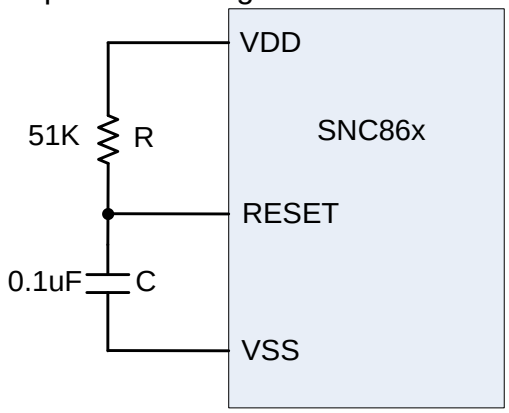
7.5. Reset Functions

There are three ways in which a device reset can occur through events occurring both internally and externally:

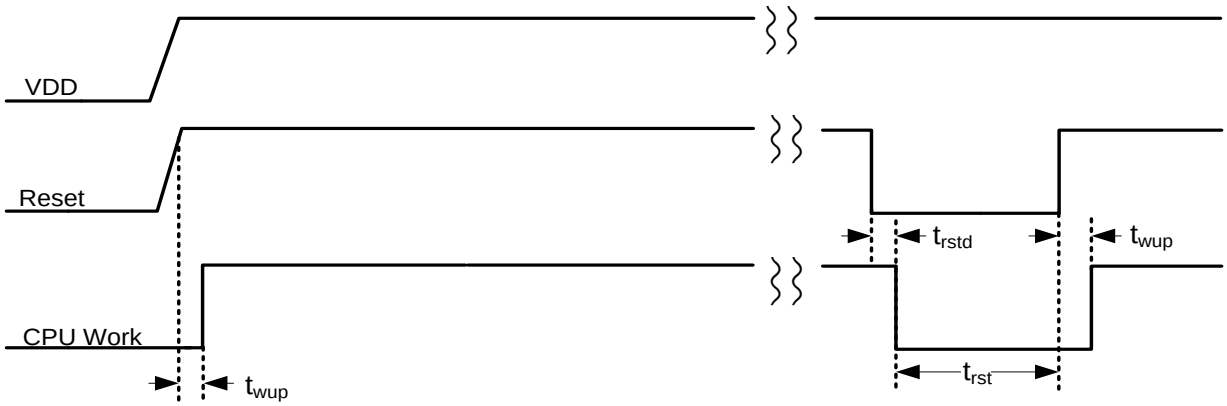
- **Power-on Reset**

The most fundamental and unavoidable reset is the one that occurs when power is first applied to the microcontroller. As well as ensuring that the Program Memory begins execution from the first memory address, a power-on reset also ensures that certain other registers are preset to known conditions. All the I/O port and port control registers will power up in a high condition ensuring that all pins will be first set to inputs.

The SNC86KC power-on reset occurs through an external RC reset circuit and onto the RESET input. The power-on reset circuit holds the device in Reset until VDD has reached an acceptable level for minimum operation voltage.



Basic Reset Circuit



Power On and Reset Timing

Symbol	Description	Min.	Typ.	Max.	Unit
t_{wup}	CPU warm up time	0.2			ms
t_{rst}	CPU reset time	3			ms
t_{rstd}	CPU reset de-bounce time	0.2			ms

- **Low Voltage Reset**

The SNC86KC contains a Low Voltage Reset (LVR) circuit in order to monitor the supply voltage of the device. If the supply voltage of the device drops to less than 2.0V, the LVR will automatically reset the device internally. If the low voltage state does not exceed 200us, the LVR will be ignored and will not perform a reset function.

- **Watch Dog Reset**

The device contains an internal Watch Dog Timer (WDT). This Watchdog timer issues a reset signal to the chip if it is not cleared before reaching a terminal count. **The watchdog timer is enabled at reset and cannot be disabled**.

7.6. Interrupts

Interrupts are an important part of any microcontroller system. The SNC86KC provides 11 interrupt sources. When the CPU enters an interrupt service routine, the GIE bit (in INTEN) will be cleared to "0". Any other interrupt requests will not be granted at this time. Instead, these requests will be queued in INTRQ.*IRQ, and will be served once GIE is restored to "1" The GIE will be restored to 1 once the CPU exits an ISR.

Interrupt vectors table:

Interrupt Source	Priority	Entry Location	Descriptions
TimerA	1	0X10	TimerA interrupt
-	2	0x14	reserved
TimerB	3	0x18	TimerB interrupt
INT0	4	0x1C	External INT0
INT1	5	0x20	External INT1
PWMIO	6	0x24	PWMIO Counter
TimerC	7	0x28	TimerC interrupt
INT2	8	0x2C	External INT2
Timer1	9	0x30	Timer1 interrupt
-	10	0x34	reserved
CMP	11	0x38	Comparator edge trigger
TimerD	12	0x3C	Timer D interrupt for Cap sensing
-	13	0x40	reserved
-	14	0x44	reserved
RTC	15	0x48	RTC interrupt

7.7. Wave Processing Unit

The SNC86KC provides two ways to play voice/sound. The first way is by 24 channel hardware channel and the second by 14-bit software.

The hardware channel is built-in the Wave Processing Unit. It is a high-performance multi-channel music synthesizer to provide high-quality wave-table melody playback. Many events of the standard MIDI file format are supported by a MIDI to Melody converter software tool.

The major function of wave synthesizer is to synthesis wave data from ROM area into voice. It is equipped with sampling rate counter, auto repetition function, and envelope control for each individual channel. With the help of the wave synthesizer, playing multi-channel music can be realized with little software effort.

The voice/sound algorithms support 5-bit ASDPCM, 6-bit ASDPCM, 8-bit ASDPCM and 12-bit ASDPCM compression format.

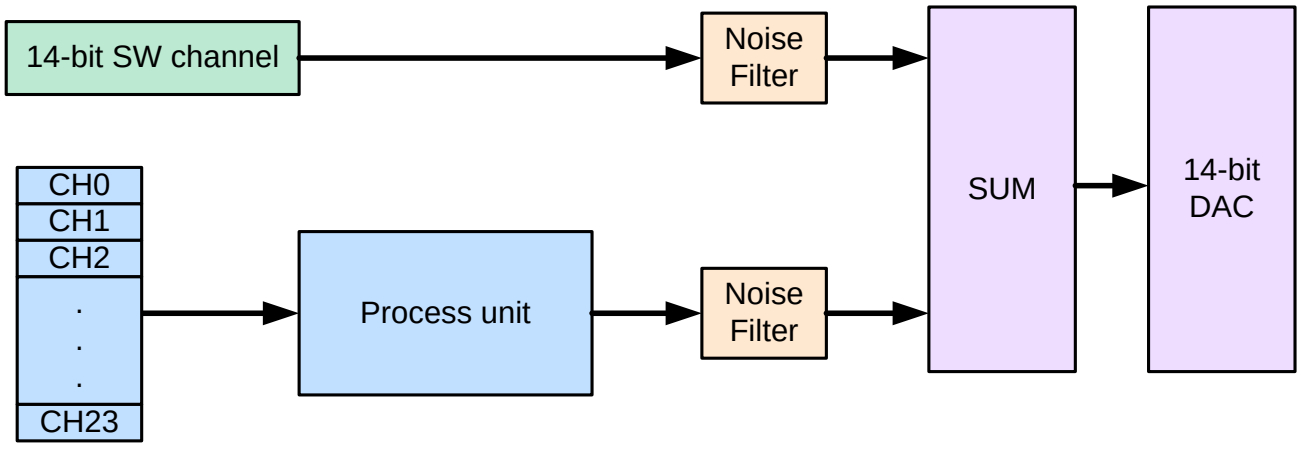
Wave Mark to trigger event in program is also supported.

The 14-bit software channel with SONiX HQDPCM algorithm is provided for high-quality sound and supports 4-bit HQDPCM or 5-bit HQDPCM to play voice/sound.

For better sound quality, the hardware channel and 14-bit high-quality software channel both include a noise filter.

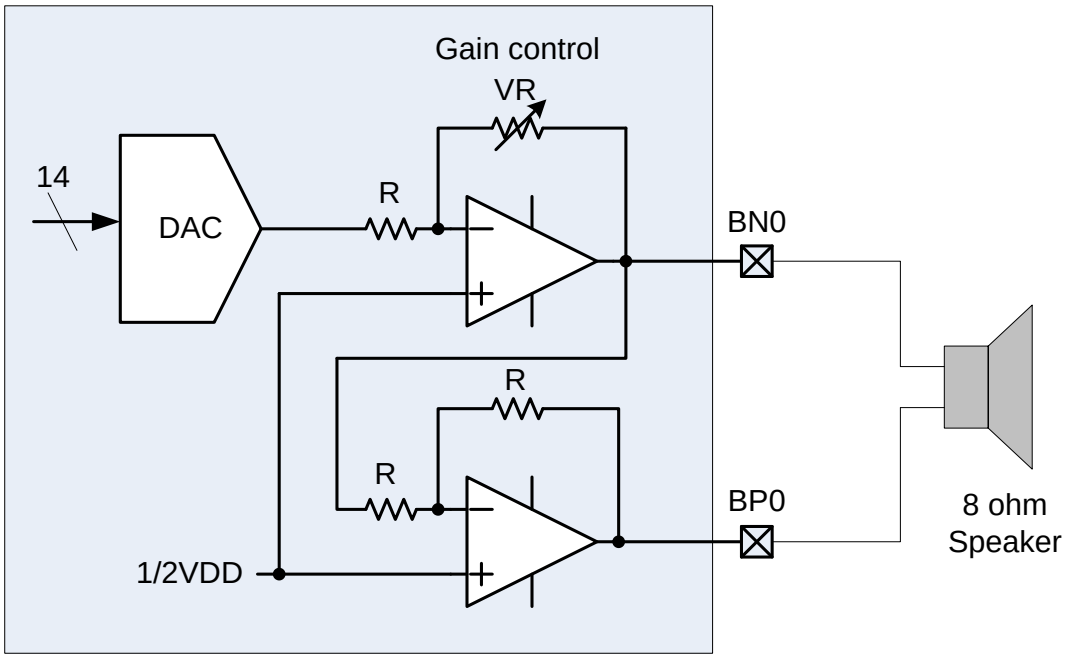
WPU	Channel Number (Max.)	Encode Type	Up-Sampling Filter	Sample Rate (Max).	Application
HWCH	24	5,6,8,12bit ADPCM	1,2,4X	48khz	Midi
SWCH	1	4,5bit HQADPCM	1,2,4X	20khz	Speech
	2	4,5bit HQADPCM	1,2,4X	16khz	Speech

Wave Processing Unit structure.



7.8. DAC with Push-Pull Amplifier

All SNC86KC series devices include a high quality 14-bit DAC with Push-Pull amplifier that will directly drive an 8 ohm speaker without requiring any external components. The Push-Pull DAC internally includes a 64-level gain control making it easy to control output volume.



Push-Pull DAC Architecture

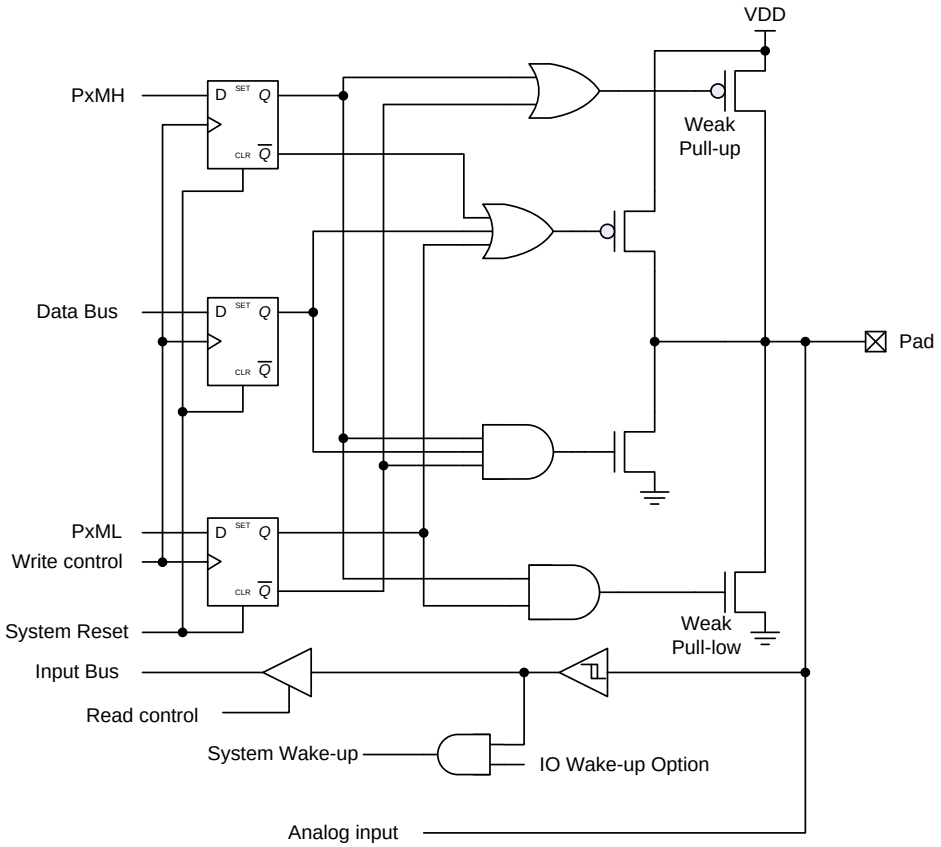
7.9. Input / Output Ports

The SNC86KC offers considerable flexibility on the I/O ports. With the input or output designation of every pin fully under program control, pull-low / pull-high / floating options for all ports and provide wake-up function on all pins, the SNC86KC has an I/O structure to meet the needs of a wide range of application possibilities.

Depending upon which device or package is chosen, the SNC86KC provides from 16 to 32 bidirectional input/output lines labeled with port names P0, P1, etc. All of these I/O ports can be independently used for input and output operations and functions. Part of the I/O port provides high drive/sink currents that can directly drive an LED without requiring any external components.

I/O port supports four configurations for all GPIO:

PxMH	PxML	Port Mode
PxMH[n] = 0	PxML[n] = 0	Px.n as Input pull low (default)
PxMH[n] = 0	PxML[n] = 1	Px.n as Input pull high
PxMH[n] = 1	PxML[n] = 0	Px.n as Output
PxMH[n] = 1	PxML[n] = 1	Px.n as Input floating



Input / Output Port Structure

- **Input Pull-Low / Pull-High / Floating**

Many product applications require pull-low or pull high resistors for their switch inputs, usually requiring the use of an external resistor. To eliminate the need for these external resistors, all I/O pins, when configured as an input have the capability of being connected to an internal pull-low or pull-high resistor. Each individual input of I/O ports pull-low resistor, pull-high resistor or floating options settings are by register control.

- **Port Wake-up**

The SNC86KC has a Sleep/Idle mode by instruction enabling the microcontroller to enter a power saving operating mode, a feature that is important for battery and other low-power applications. Any transition, low to high or high to low, on an input pin will wake the CPU into normal operating mode.

7.10. Multi-Function of I/Os

The flexibility of the microcontroller range is greatly enhanced by the use of pins that have more than one function. Limited numbers of pins can force serious design constraints on designers however by supplying pins with multiple functions, many of these difficulties can be overcome. For some pins, the chosen function of the multi-function I/O pins is set by configuration options while for others, the function is set by application program control.
A summary of I/O multi-function is shown below.

IO \ Function	CMP0		EX-INT	SPI	PWMIO	IR	High drive/sink	XTAL
P0.00	[0]							Xin
P0.01	[1]							Xout
P0.02	[2]			CS				
P0.03	[3]			SCK				
P0.04	[4]			DO/D0				
P0.05	[5]			DI/D1				
P0.06	[6]			D2				
P0.07	[7]			D3				
P0.08	[8]				[0]		V	
P0.09	[9]				[1]		V	
P0.10	[10]				[2]		V	
P0.11	[11]				[3]		V	
P0.12	[12]		INT0		[4]		V	
P0.13	[13]		INT1		[5]		V	
P0.14	[14]		INT2		[6]		V	
P0.15	[15]				[7]	V	V	
P1.00	[16]	IN(+)			[8]		V	
P1.01	[17]	OUT(o)			[9]		V	
P1.02	[18]				[10]		V	
P1.03	[19]				[11]		V	
P1.04	[20]						V	
P1.05	[21]						V	
P1.06	[22]						V	
P1.07	[23]					V	V	
P1.08	[24]							
P1.09	[25]							
P1.10	[26]							
P1.11	[27]							
P1.12	[28]							
P1.13	[29]							
P1.14	[30]							
P1.15	[31]							

Note: (1) Different chip bodies have different number of I/O.

7.11. Timers

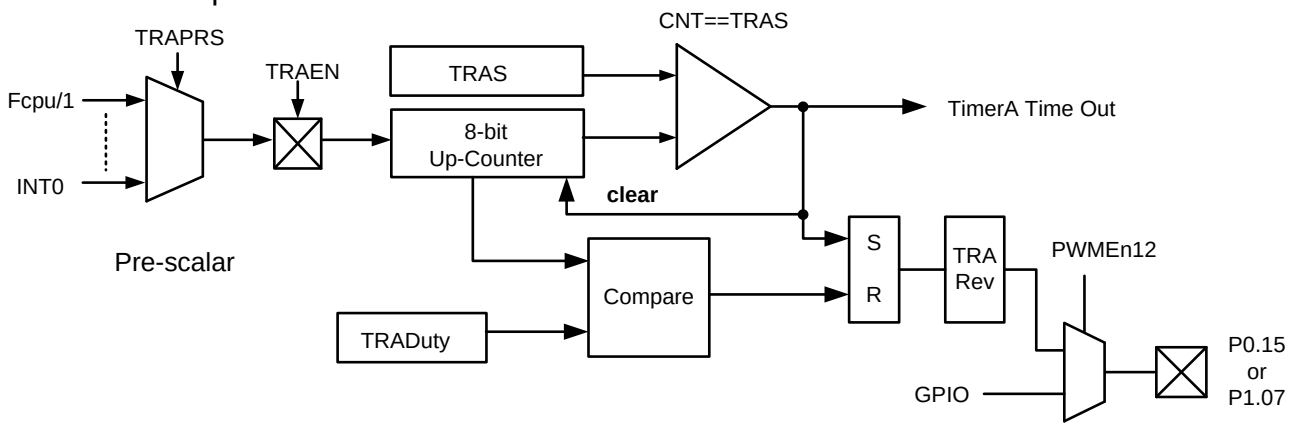
The provision of timers form an important part of any microcontroller giving the program designer a means of carrying out time related functions. The SNC86KC series contains one 8-bit count up timer, two 12-bit count up timers, and a selectable 1ms / 4ms fixed timer providing for flexible applications where many timers required.

7.11.1 TimerA (8-bit counter/timer)

TimerA is a special timer. It is an 8-bit binary up-counting timer with auto-reload function or event counter function, as well as perform IR and PWM output functions. If a successful event occurs (counting value = set value), it will issue a time out signal to TimerA interrupt service and continue counting.

TimerA features:

1. 8-bit up counter with interrupt function.
2. External interrupt 0 (INT0) counter.
3. IR modulation. Duty cycle can be programmable 1/2, 2/3, 1/3, 1/4.
4. PWMIO output.



TRA: TimerA Control Register

BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
TRA (0x3C)	T1CLR	T1TO	T1TOS	TRAEN	TRAAR	TRAPRS[2:0]		
R/W	C1	R/C0	R/W	R/W	R/W	R/W		
default	0	0	0	0	0	000		
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	TRAS[7:0]							
R/W	R/W							
default	0000,0000							

TRAEN: TimerA enable
0: disable
1: enable

TRAAR: TimerA auto reload
0: disable auto reload
1: enable auto reload

TRAPRS[2:0]: TimerA pre-scale

TRAPRS[2:0]		Fcpu: 6144KHz
000b	Fcpu/1	6144KHz
001b	Fcpu/2	3022KHz
010b	Fcpu/8	768KHz
011b	Fcpu/64	96KHz
100b	Fcpu/256	24KHz
101b	source from external INT0	
110b	Reserve	
111b	Reserve	

TRAS[7:0]: TimerA up-count set value.
Write: set counting limit value
Read: current up-counting value

The TRAS register records TimerA counter value, which can control time-out time of TimerA. When TRAEN=1, TimerA will start counting from 0 to this counting limit value. If a successful event occurs (counting value = limit value), it will restart counting and issue a time out signal(INTRQ – interrupt request). If TRAINTEN=1 and GIE=1, it will enter TimerA interrupt service routine.

Note. Writing zero into TRAS[7:0] register is prohibited.

TRAPWM: PWMIO or IR Control Register

BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
TRAPWM (0x3C)	Reserved					PWMIO12S	PWMIO12EN	PWMIO12REV
R/W	-					R/W	R/W	R/W
default	00000					0	0	0
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	DUTY[7:0]							
R/W	R/W							
default	0000,0000							

PWMIO12S: PWMIO12 output select
0: PWM/IR output on P0.15
1: PWM/IR output on P1.07

PWMIO12EN: PWMIO12 or IR enable
0: Disable (Normal GPIO)

1: PWMIO12 or IR output enable

PWMIO12REV: PWMIO12 Output Reverse
0: Normal
1: PWMIO12 Output Reverse

Duty[7:0]: PWMIO12 duty register

IR Output Configuration

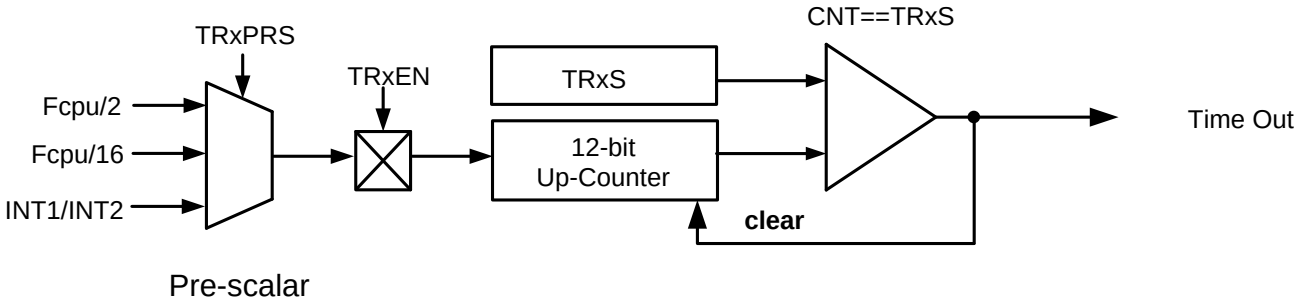
TRAPRS[2:0]	TRAS[7:0]	IR freq	DUTY[7:0]		
			1/2 duty	2/3 duty	1/3 duty
000b (Fcpu/1)	160	38.4KHz	80	106	53

7.11.2 TimerB/TimerC (12-bit counter/timer)

TimerB and TimerC are general-purpose timers. Each is a 12-bit binary up-counting timer with auto-reload or event counter function. If a successful event occurs (counting value = set value), it will issue a time out signal to TimerB and TimerC interrupt service and continue counting. CPU clock or external clock can be selected to be timer's clock source.

The TimerB and TimerC features include as below,

1. 12-bit up counter with interrupt function.
2. External interrupt (INT1/INT2) counter.



BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
TRx	TRxEN	TRxAR	TRxPRS[1:0]		TRxS[11:8]			
R/W	R/W	R/W	R/W		R/W			
default	0	0	00		0000			
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	TRxS[7:0]							
R/W	R/W							
default	0000,0000							

TRxEN: TimerB/C enable
0: disable
1: enable
TRxAR: TimerB/C auto reload
0: disable auto reload
1: enable auto reload
TRxPRS[1:0]: Timerx pre-scale

TRxPRS[1:0]		Fcpu: 6144KHz
00b	Fcpu/2	3072KHz
01b	Fcpu/16	384KHz
1Xb	source from external INT1	

TRxS[11:0]: TimerB/C count value

Write: set counting limit value

Read: current up-counting value

When counting value = set value, up-counter will auto-reload. Maximum is 4095.
Note. Writing zero into TRxS[11:0] register is prohibited.

7.11.3 Timer1

Timer1 is a special timer that provides either 4ms or 1ms time out flag. The timer also has its own interrupt service(vector).

BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
TRA (0x3C)	T1CLR	T1TO	T1TOS	TRAEN	TRAAR	TRAPRS[2:0]		
R/W	C1	R/C0	R/W	R/W	R/W	R/W		
default	0	0	0	0	0	000		
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	TRAS[7:0]							
R/W	R/W							
default	0000,0000							

T1CLR: Clear Timer1 count

Write T1Clr with 1 to clear the counting value. The T1CLR is write only and reads “0”.

T1TO: Timer1 timeout flag

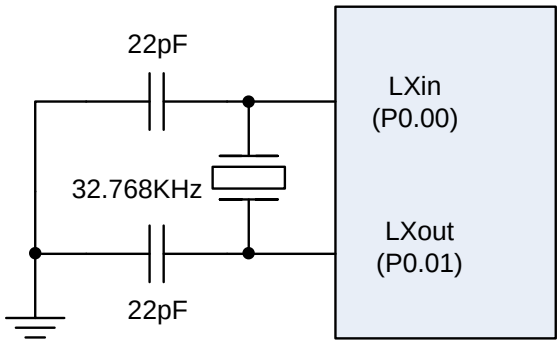
T1TO=1: Timer 1 time out. Write 0 clears this time out flag. Care must be taken when writing to other bits of this register and masked with a “1” to avoid clearing this flag unintentionally.

T1TOS: Timer1 timeout select

0: 1ms
1: 4ms

7.11.4 Real Time Clock (RTC)

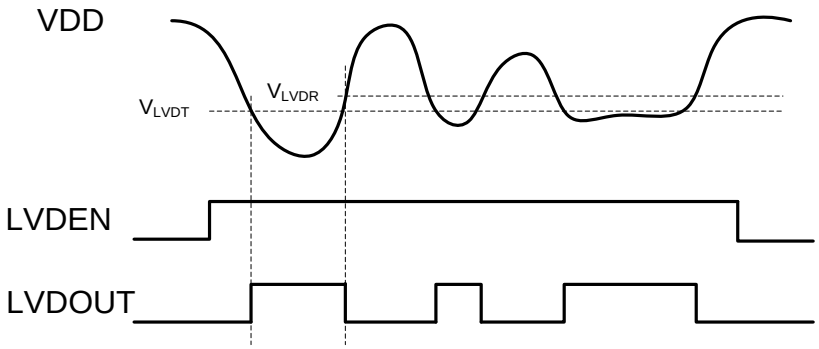
The SNC86KC has a built-in 32.768KHz oscillator circuit for Real Time Clock (RTC) function. The RTC timer provides an accurate timer for digital clock use. A 32.768KHz crystal should be connected to XTAL by shared IO inputs P0.00 and P0.01. In IDLE mode, the chip will wake up for a regular interval time by RTC timer set. RTC timer range selections of between 62.5ms and 64sec are supported.



32.768K X'tal circuit

7.12. Low Voltage Detector (LVD)

The SNC86KC has a Low Voltage Detector (LVD) for power management. This feature is favorable to product battery life requirements and can be an effective management of system power. The device provides 4 software programmable voltage levels to detect low voltage events 2.2V/2.4V/2.8V/3.2V The LVD function compares the power supply voltage VDD, with a pre-specified voltage level stored in the register. When the power supply voltage VDD falls below this pre-determined value, the LVDOUT bit will be set high indicating a low power supply voltage condition. When the device is powered down the low voltage detector will remain active if the LVDEN bit is high.



LVD Operation

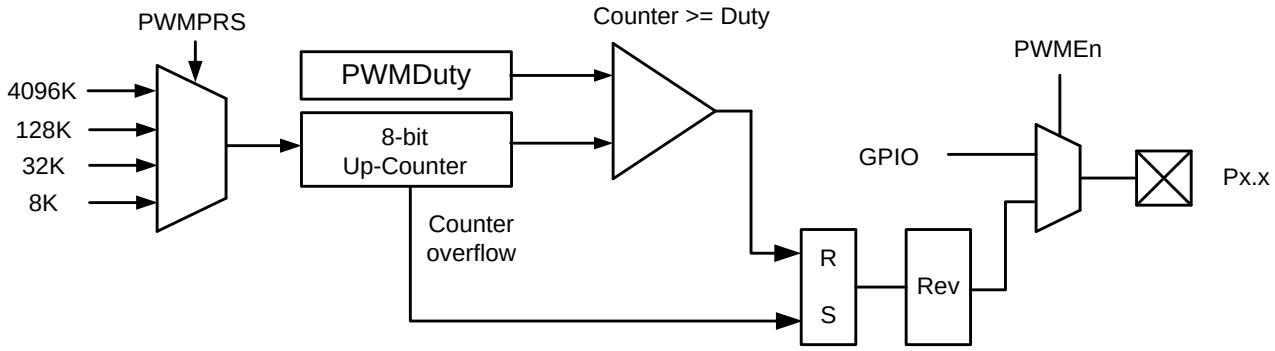
Note the LVD detect has a voltage window of about 0.1V. When LVD level = 2.4V, and VDD supply falls lower than 2.4V, the LVD will trigger LVD (V_{LVDT}). When VDD supply rises higher than 2.5V, LVD (V_{LVDR}) will be released. The LVD function does not operate in sleep or idle modes and is recommended to turn off the LVD function in these modes to reduce power consumption.

7.13. External Interrupt

The SNC86KC provides three external interrupt I/O functions on P0.12, P0.13 and P0.14. Each external interrupt provides three trigger modes: rising edge trigger, falling edge trigger and both edge trigger by software control. The external I/O can also be routed through TimerA, B and C counter to handle external trigger event counting or timing.

7.14. Pulse Width Modulation (PWMIO)

The SNC86KC supports up to 12 PWMIOs. Each I/O has an 8-bit independent duty register. The clock source of PWMIO is selected by PWMPRS[1:0] which provides 4096KHz, 128KHz, 32KHz, or 8KHz frequencies. Each PWMIO provides high drive/sink currents that can directly drive an LED without requiring external components.



BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PWMCR (0x40)	PWMCLR	BIT_REV	PWMPRS[1:0]		PWMEn11	PWMEn10	PWMEn9	PWMEn8
R/W	C0	R/W	R/W		R/W	R/W	R/W	R/W
default	1	0	00		0	0	0	0
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	PWMEn7	PWMEn6	PWMEn5	PWMEn4	PWMEn3	PWMEn2	PWMEn1	PWMEn0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
default	0	0	0	0	0	0	0	0

PWMEn0~11: PWMIO0~11 enable/disable control

0: disable

1: enable

PWMPRS[1:0]: PWMIO clock pre-scalar

PWMPRS[1:0]	PWMIO Clock Source	PWMIO Cycle
00b	0.244us (4096KHz)	62.5us (16KHz)
01b	7.8125us (128KHz)	2ms (500Hz)
10b	31.25us (32KHz)	8ms (125Hz)
11b	125us (8KHz)	32ms (31.25Hz)

PWMCLR: PWMIO counter clear

Write 0 to clear the PWM counter

Always read 1

BIT_REV: PWMIO output inverted

0: Normal

1: PWM output inverted

■ **PWMIO Duty Register**

Each PWMIO has an individual register (PWMDutyx) to set the duty. The PWM IO re-loads the data only at counter initialization.

BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PWMD0 (0x41)	**PWMDuty1[7:0]**							
R/W	**R/W**							
default	**00000000**							
BIT	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	PWMDuty0[7:0]							
R/W	**R/W**							
default	**00000000**							

BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PWMD1 (0x42)	**PWMDuty3[7:0]**							
R/W	**R/W**							
default	**00000000**							
BIT	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	PWMDuty2[7:0]							
R/W	**R/W**							
default	**00000000**							

BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PWMD2 (0x43)	PWMDuty5[7:0]							
R/W	R/W							
default	00000000							
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	PWMDuty4[7:0]							
R/W	R/W							
default	00000000							

BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PWMD3 (0x44)	PWMDuty7[7:0]							
R/W	R/W							
default	00000000							
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	PWMDuty6[7:0]							
R/W	R/W							
default	00000000							

BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PWMD4 (0x45)	PWMDuty9[7:0]							
R/W	R/W							
default	00000000							
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	PWMDuty8[7:0]							
R/W	R/W							
default	00000000							

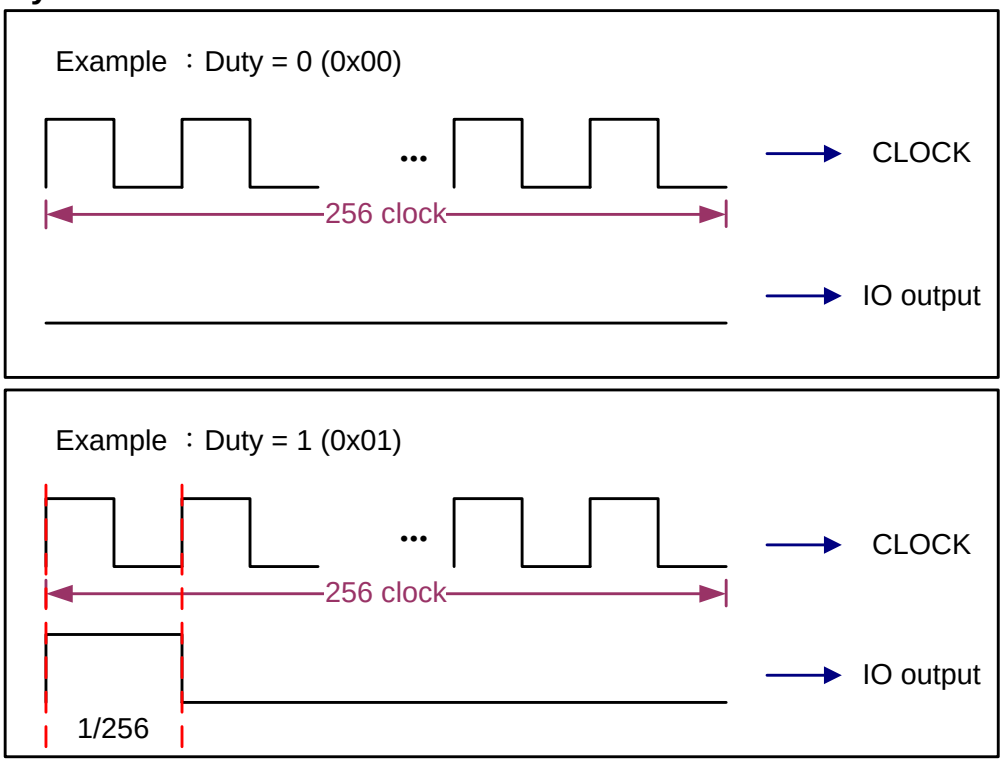
BIT	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PWMD5 (0x46)	PWMDuty11[7:0]							
R/W	R/W							
default	00000000							
BIT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	PWMDuty10[7:0]							
R/W	R/W							

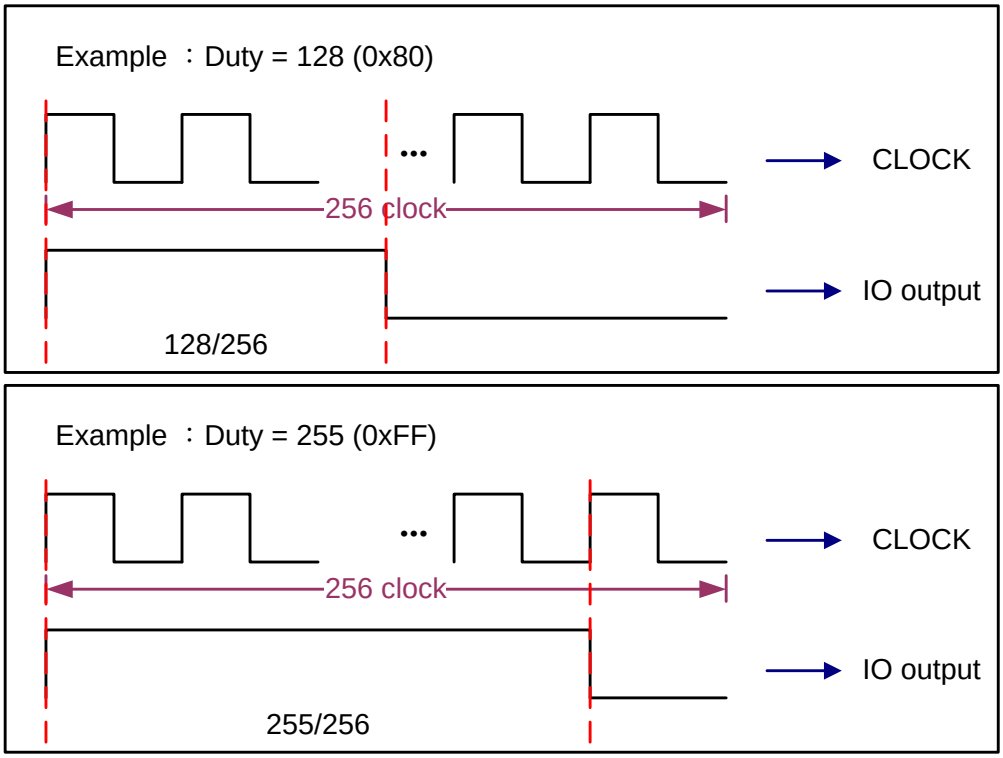
default	00000000

16 / 24 / 32 IO body PWMIO Register mapping

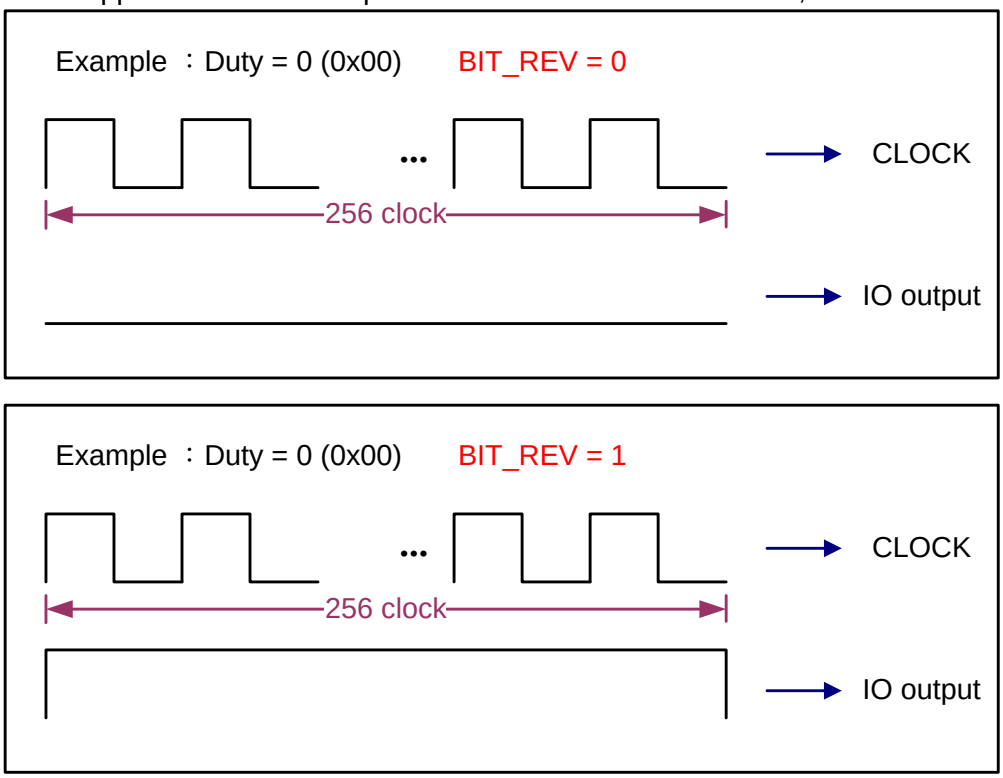
Body	Port	Enable bit	Duty
16 IO / 24 IO / 32 IO	P0.08	PWMCR.0	PWMD0[7:0] (PWMDuty0)
	P0.09	PWMCR.1	PWMD0[15:8] (PWMDuty1)
	P0.10	PWMCR.2	PWMD1[7:0] (PWMDuty2)
	P0.11	PWMCR.3	PWMD1[15:8] (PWMDuty3)
	P0.12	PWMCR.4	PWMD2[7:0] (PWMDuty4)
	P0.13	PWMCR.5	PWMD2[15:8] (PWMDuty5)
	P0.14	PWMCR.6	PWMD3[7:0] (PWMDuty6)
	P0.15	PWMCR.7	PWMD3[15:8] (PWMDuty7)
24 IO / 32 IO	P1.00	PWMCR.8	PWMD4[7:0] (PWMDuty8)
	P1.01	PWMCR.9	PWMD4[15:8] (PWMDuty9)
	P1.02	PWMCR.10	PWMD5[7:0] (PWMDuty10)
	P1.03	PWMCR.11	PWMD5[15:8] (PWMDuty11)

PWMIO Duty control:

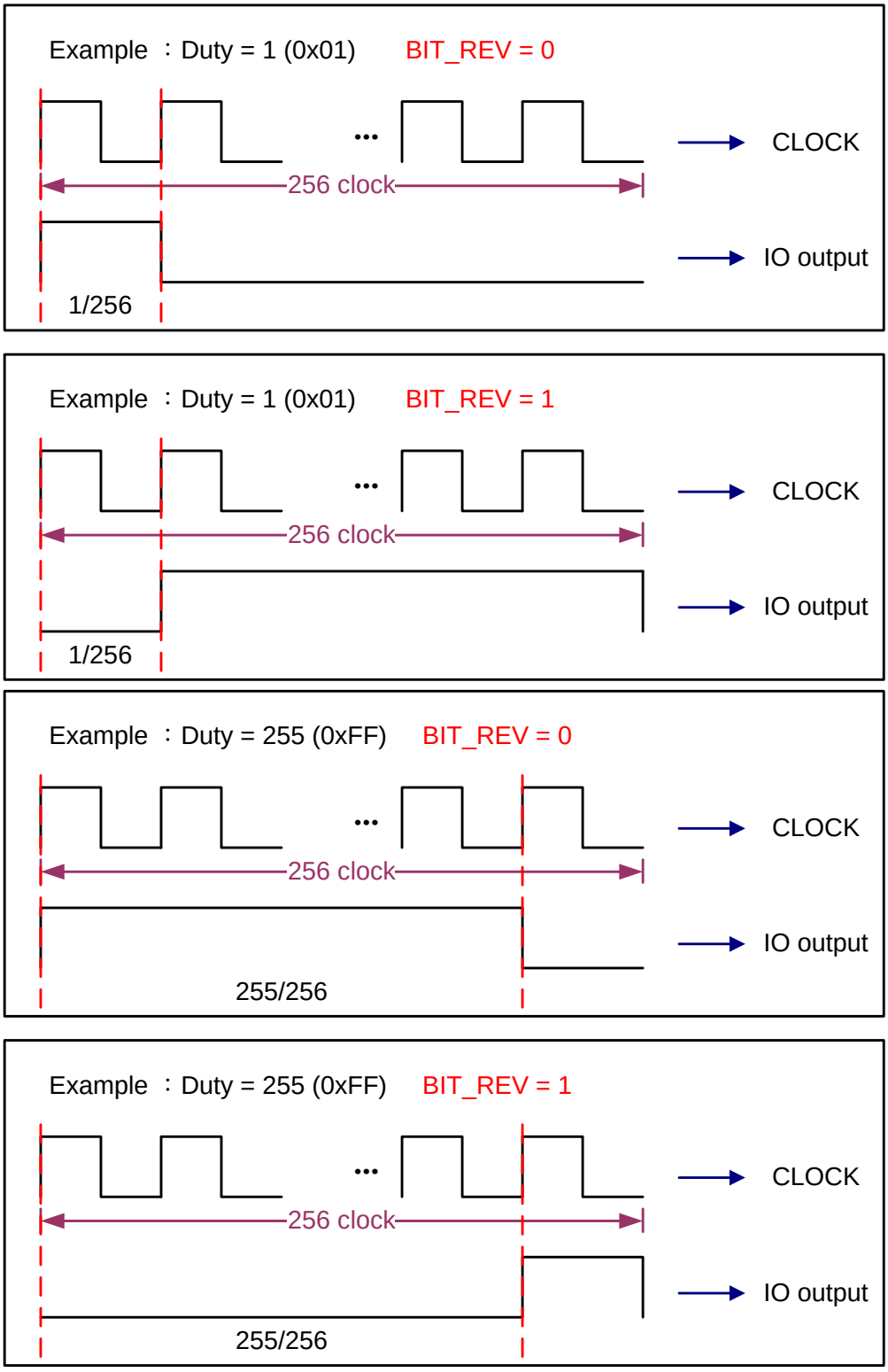




SNC86KC have support PWMIO IO output reverse. If use sink mode LED, user can set BIT_REV = 1.

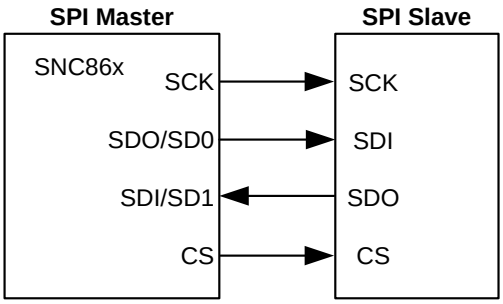


Note. Set BIT_REV = 1 and Duty = 0 to let sink mode LED completely low.

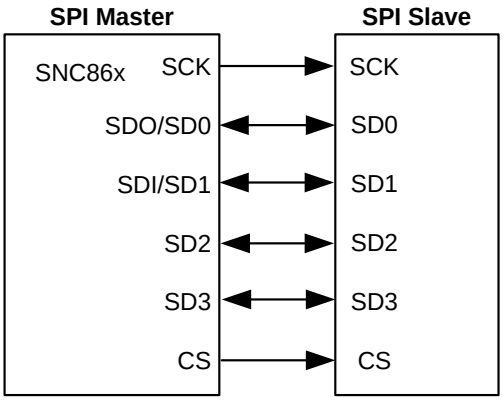

Example ：Duty = 1 (0x01) BIT_REV = 0
CLOCK
256 clock
IO output
1/256
Example ：Duty = 1 (0x01) BIT_REV = 1
CLOCK
256 clock
IO output
1/256
Example ：Duty = 255 (0xFF) BIT_REV = 0
CLOCK
256 clock
IO output
255/256
Example ：Duty = 255 (0xFF) BIT_REV = 1
CLOCK
256 clock
IO output
255/256

7.15. Serial Peripheral Interface (SPI)

The SNC86KC supports a Serial Peripheral Interface (SPI). The SPI interface is a synchronous serial data interface that has a relatively simple communication protocol simplifying the programming requirements when communicating with external hardware devices. The interface is often used to communicate with external peripheral devices such as sensors, Flash or EEPROM memory devices etc. The device supports Master mode only which can meet the requirements of a majority of applications. The SNC86KC provides standard single I/O mode or Quad I/O mode to elevate accessing external Flash or EEPROM speed. The maximum SPI clock rate is up to 6.144MHz.

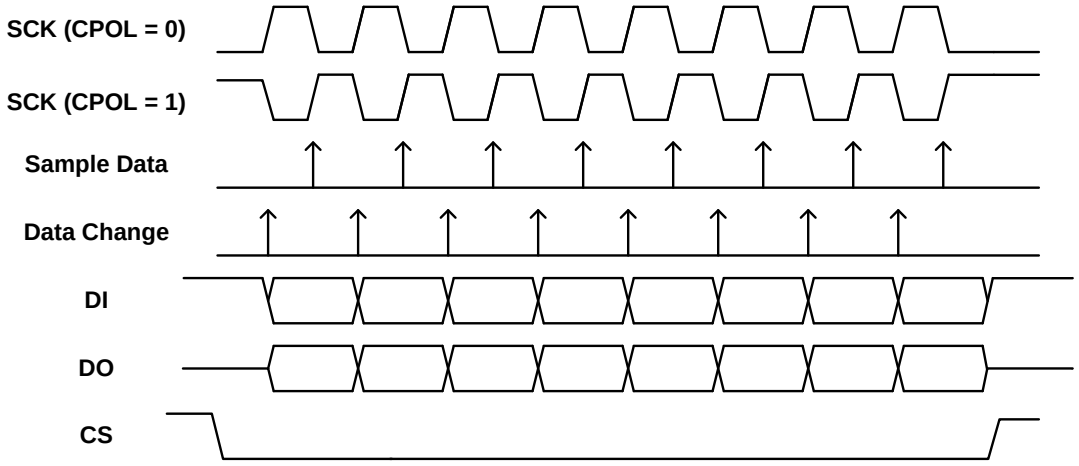


SPI Standard Mode Connection

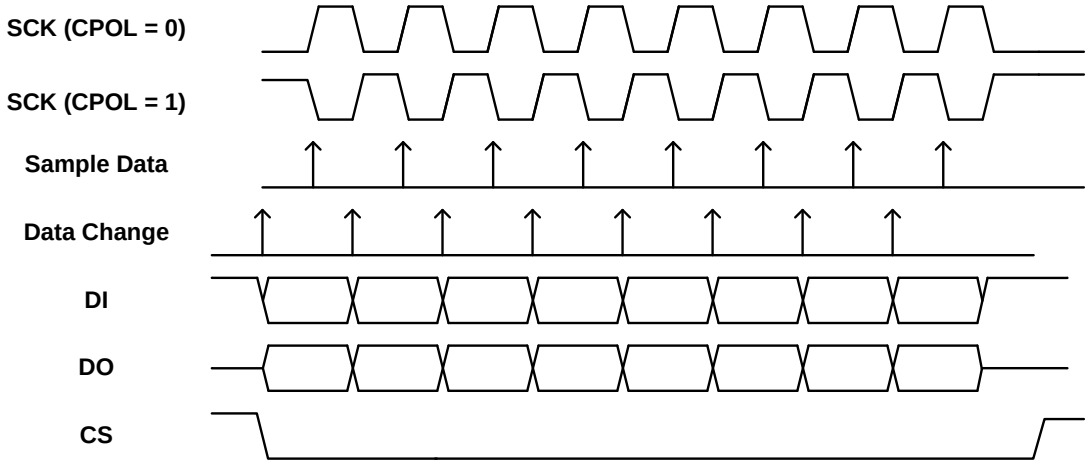


SPI Quad I/O Mode Connection

Software can select any of four combinations of serial clock (SCK) phase and polarity. The clock polarity is specified by the CPOL control bit which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. The following is an SPI transfer format with different CPOL and CPHA values.



CHPA = 1



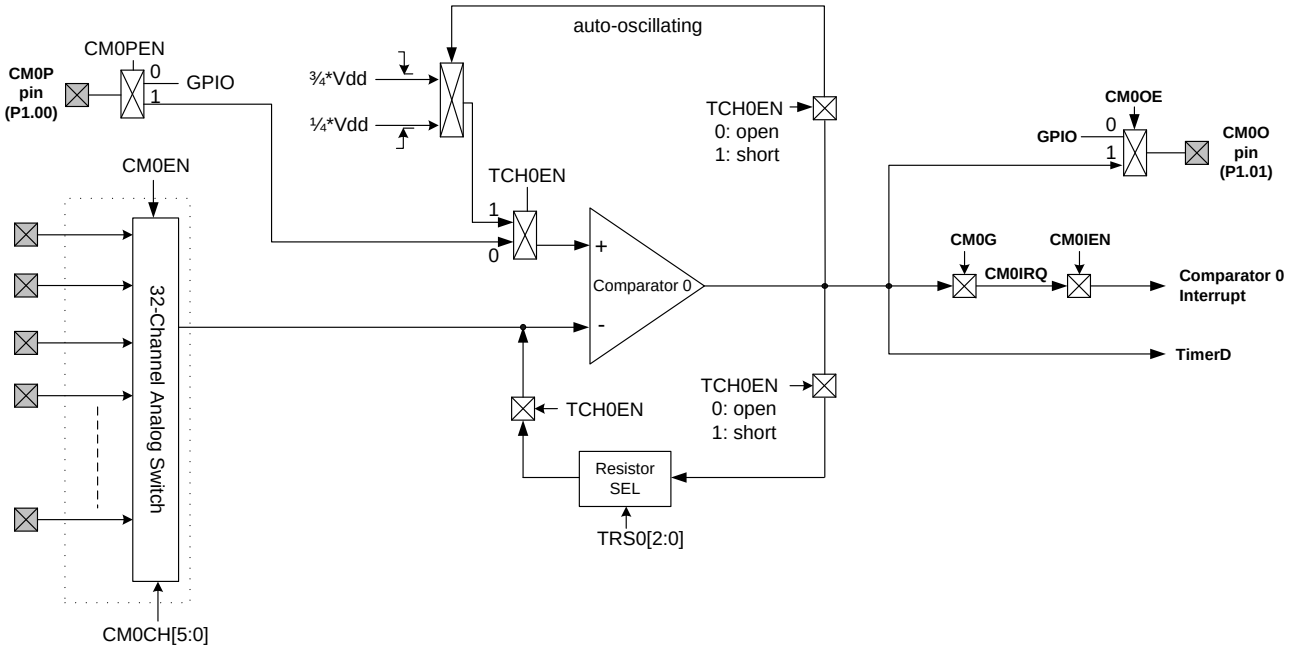
CHPA = 0

CPOL	CPHA	Function
0	0	Data is read on the clock's rising edge (low->high transition) and data is changed on a falling edge (high->low clock transition).
0	1	Data is read on the clock's falling edge and data is changed on a rising edge
1	0	Data is read on clock's falling edge and data is changed on a rising edge.
1	1	Data is read on clock's rising edge and data is changed on a falling edge.

7.16. Comparator

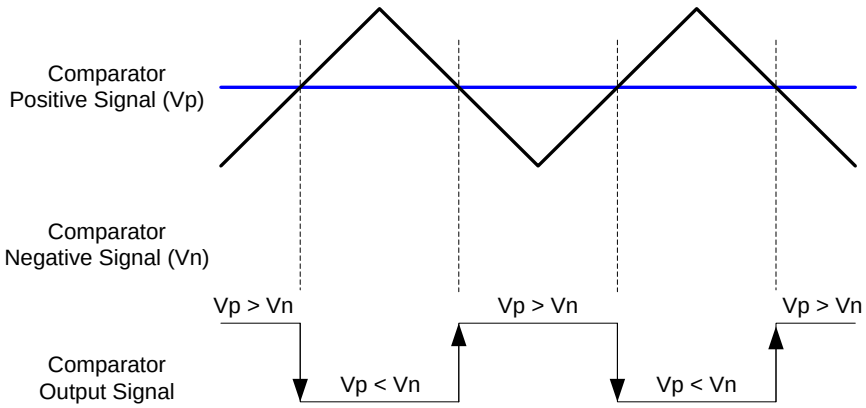
The SNC86KC includes an analog comparator function. There are 32-channel negative input pins, auto-oscillating circuit with controllable feedback resistors, as well as programmable interrupt trigger configurations. The comparator circuit operates as a normal comparator or can be configured for Cap-Sensing applications. The main parts of the 32-channel comparator circuit includes the following:

- 32-channel negative input selection.
- Comparator output function.
- Auto-oscillating control block.
- Cap-Sensing compensation.
- Interrupt function.



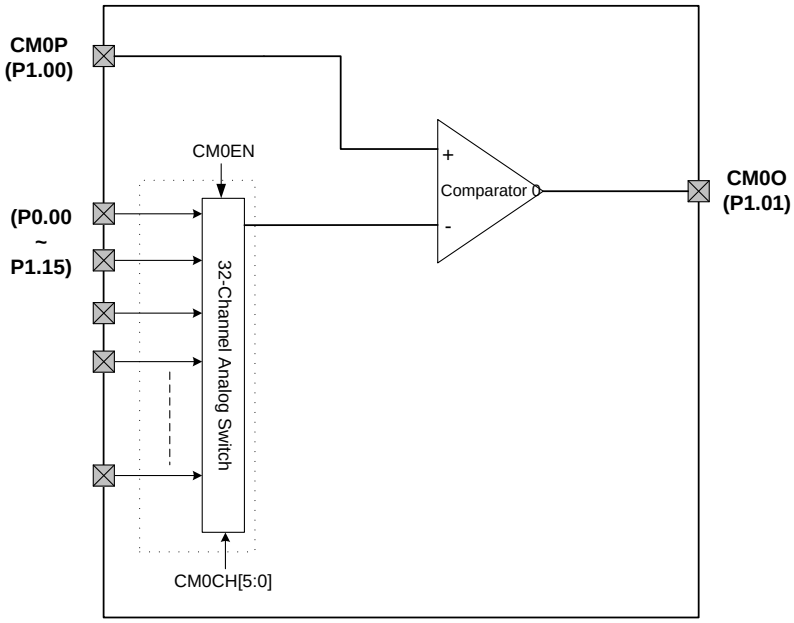
7.16.1 Comparator Operation

The comparator operation is to compare the voltage between comparator positive input and negative input terminals. When the positive input voltage is greater than the negative input voltage, the comparator output is high status. When the positive input voltage is less than the negative input voltage, the comparator output is low status.



7.16.2 Normal Comparator Configuration

The comparator function through register settings can be used as normal comparator mode. When TCH0EN=0, the comparator will disconnect the internal circuit. When CM0PEN=1 and CM0OE=1, the comparator positive input is connected to GPIO (P1.00) and the comparator output is connected to GPIO (P1.01). The comparator negative input terminals support up to a maximum of 32 channels controlled by CH0CH[5:0] analog switch selection bits.

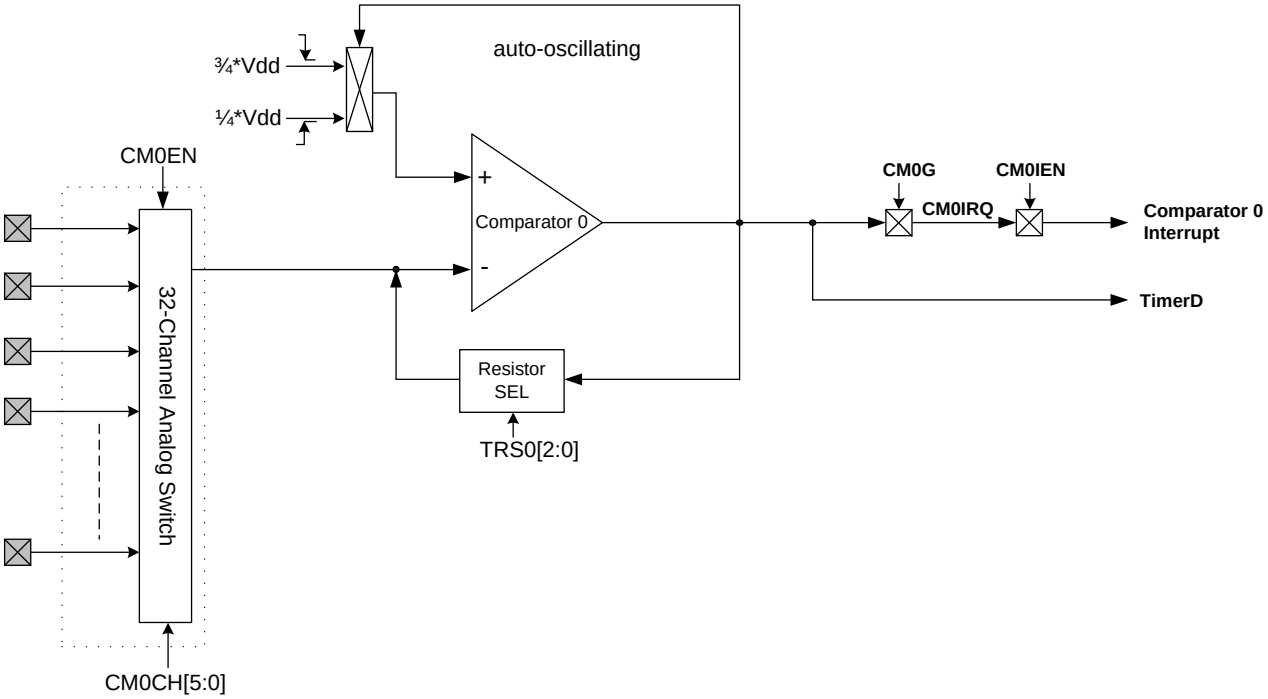


TCH0EN=0, Normal Comparator Mode

7.16.3 Cap-Sensing Configuration

The negative input terminal connects to the external input pin and auto-oscillating output terminal. When TCH0EN=1, the comparator connects to the internal auto-oscillating circuit and the positive input terminal connects to the internal reference voltage source. The comparator negative input terminal supports up to a maximum of 32 channels controlled by CH0CH[5:0] analog switch selection bits. The CM0OUT flag indicates the comparator result

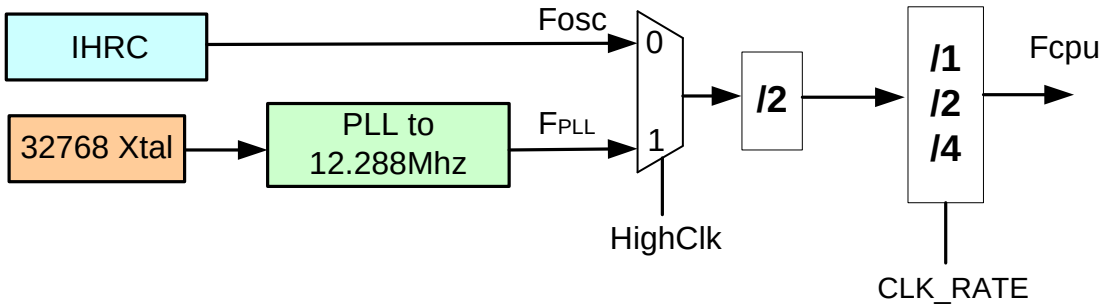
is available and immediately accessible while the CM0IRQ only indicates the event of the comparator result.



TCH0EN=1, Cap-Sensing Mode

7.17. System Clock

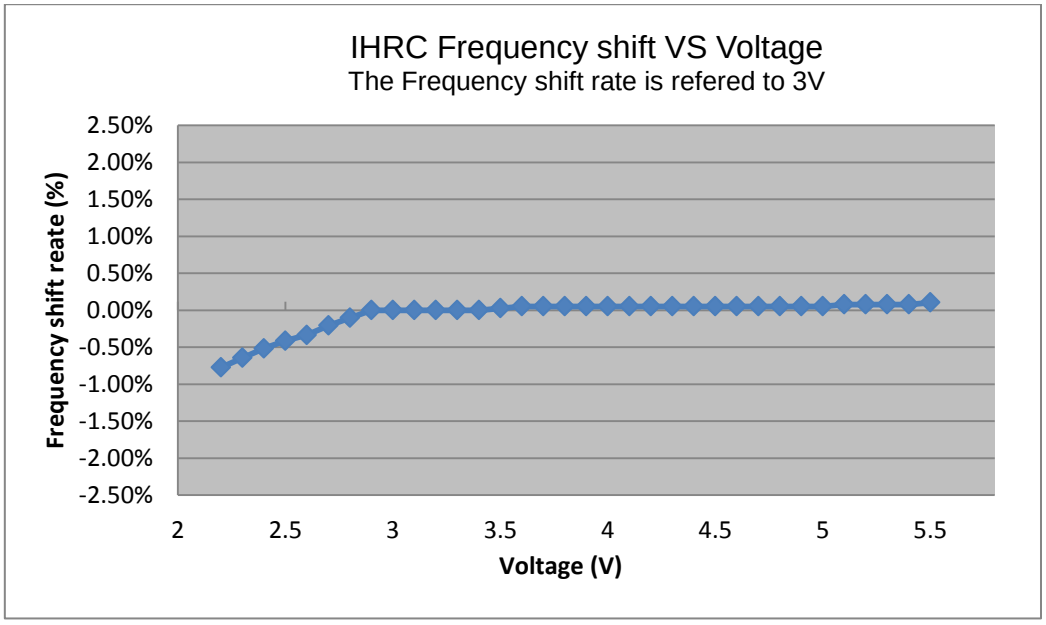
The SNC86KC supports selectable internal high-speed RC(IHRC) or external 32,768Hz crystal clock sources.



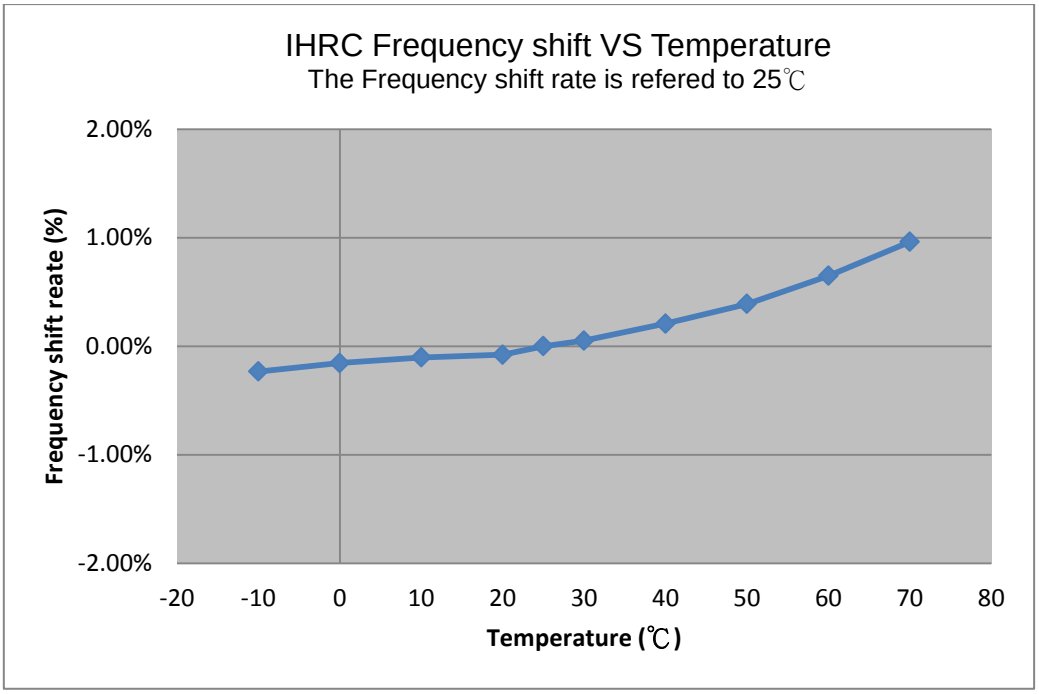
Select internal RC or Xtal system clock source

The clock structure when using a 32.768KHz crystal utilizes an internal PLL to generate high speed clock rates. The frequency accuracy is according to 32.768KHz crystal. The frequency is not affected by voltage and temperature. Applications requiring a high degree of accuracy should use this clock source that is software selectable.

IHRC frequency is affected by voltage and temperature of the system where the following illustrates the relationship.



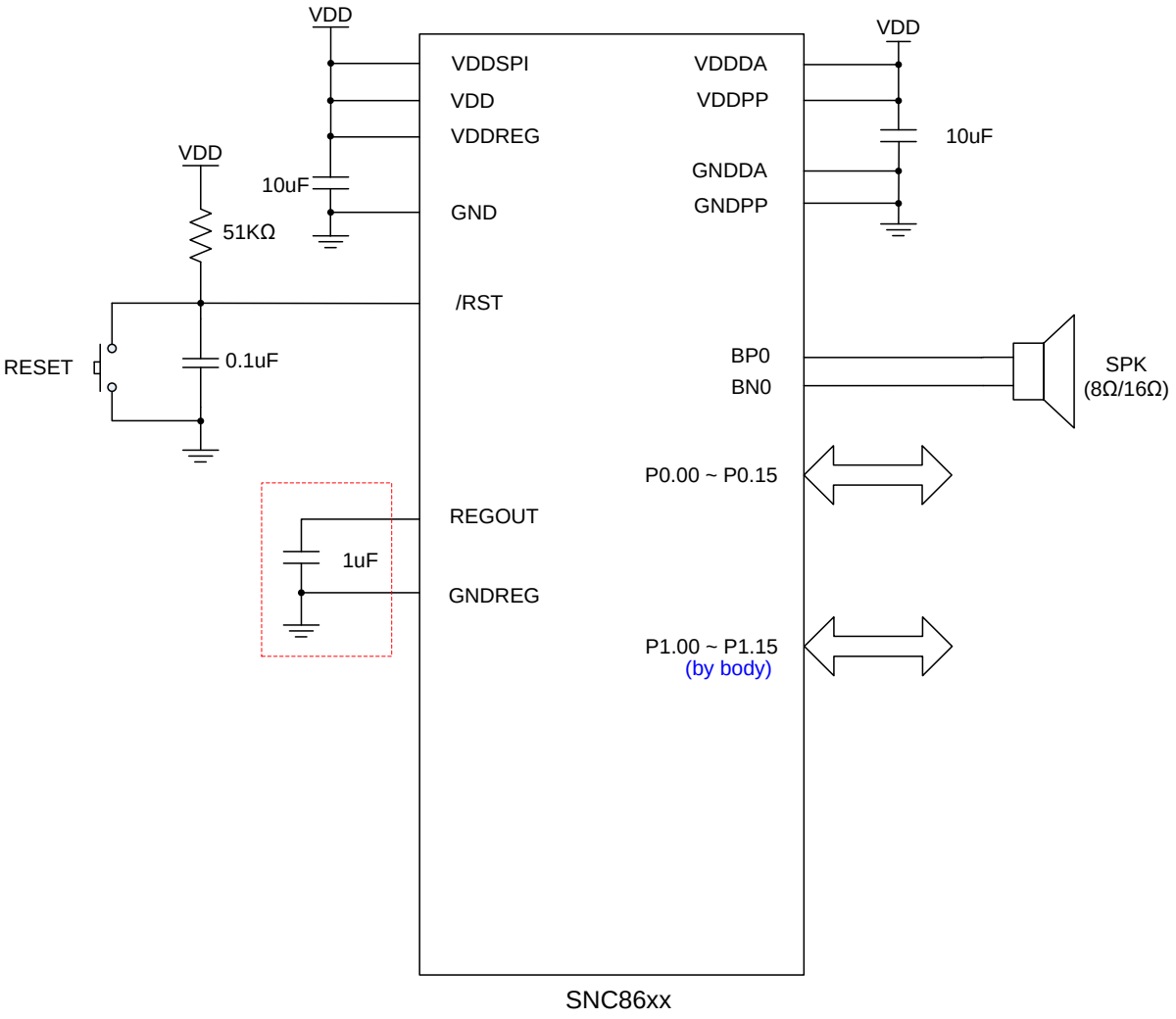
The Figure shows the relationship between high-clock frequency and temperature at VDD=3V



8 APPLICATION CIRCUIT

8.1.1 System clock from IHRC Source

Power Supply: 2.2V ~ 5.5V

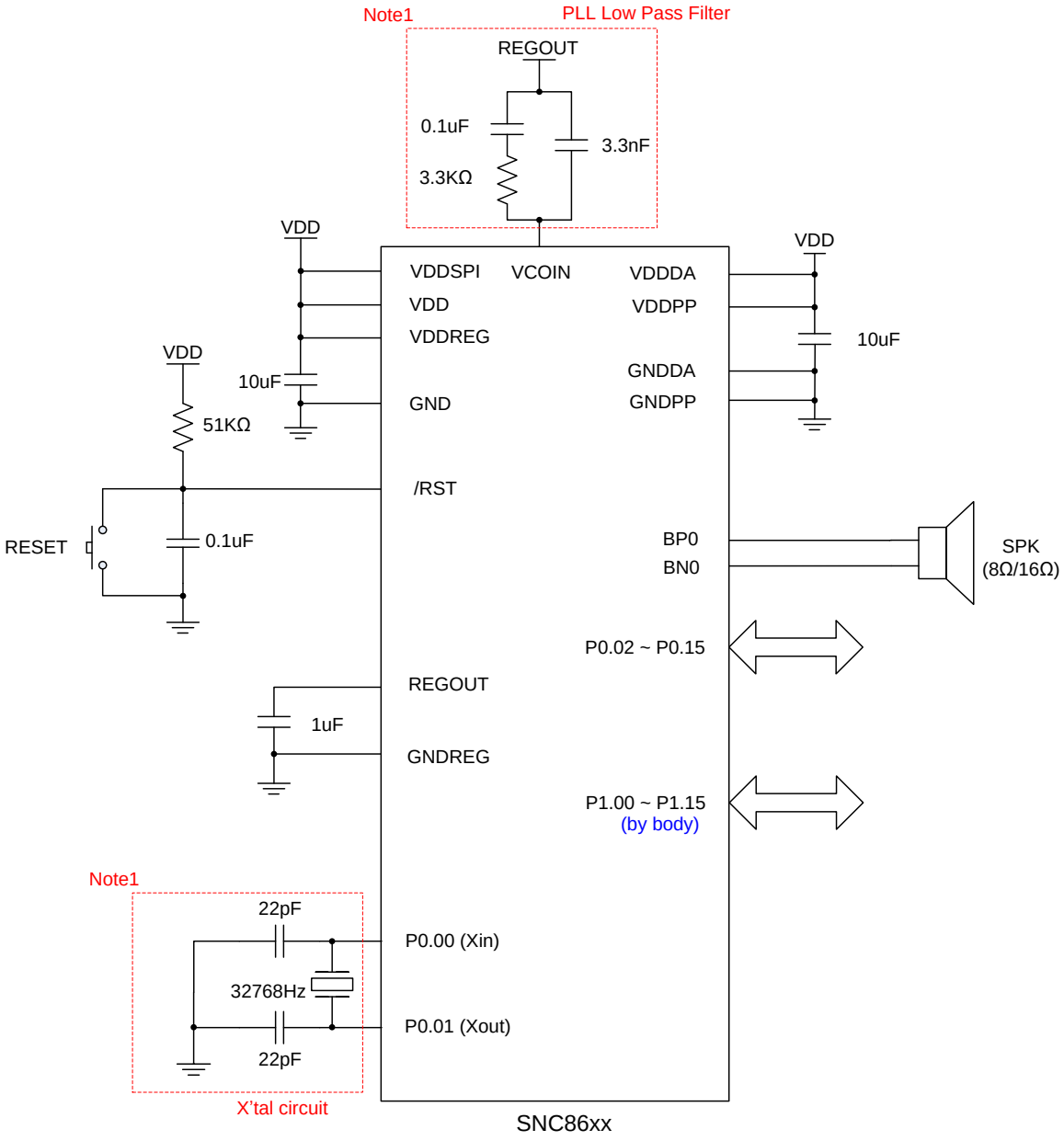


Note.

1. REGOUT pin must be connected to a 10uF capacitor for the internal regulator to work properly.
2. REGOUT PIN is regulator output pin but also for CVDD input pin.
3. VDDSPI PIN must be connected to VDD, when no SPI application.

8.1.2 System Clock from PLL Source

Power Supply: 2.2V ~ 5.5V

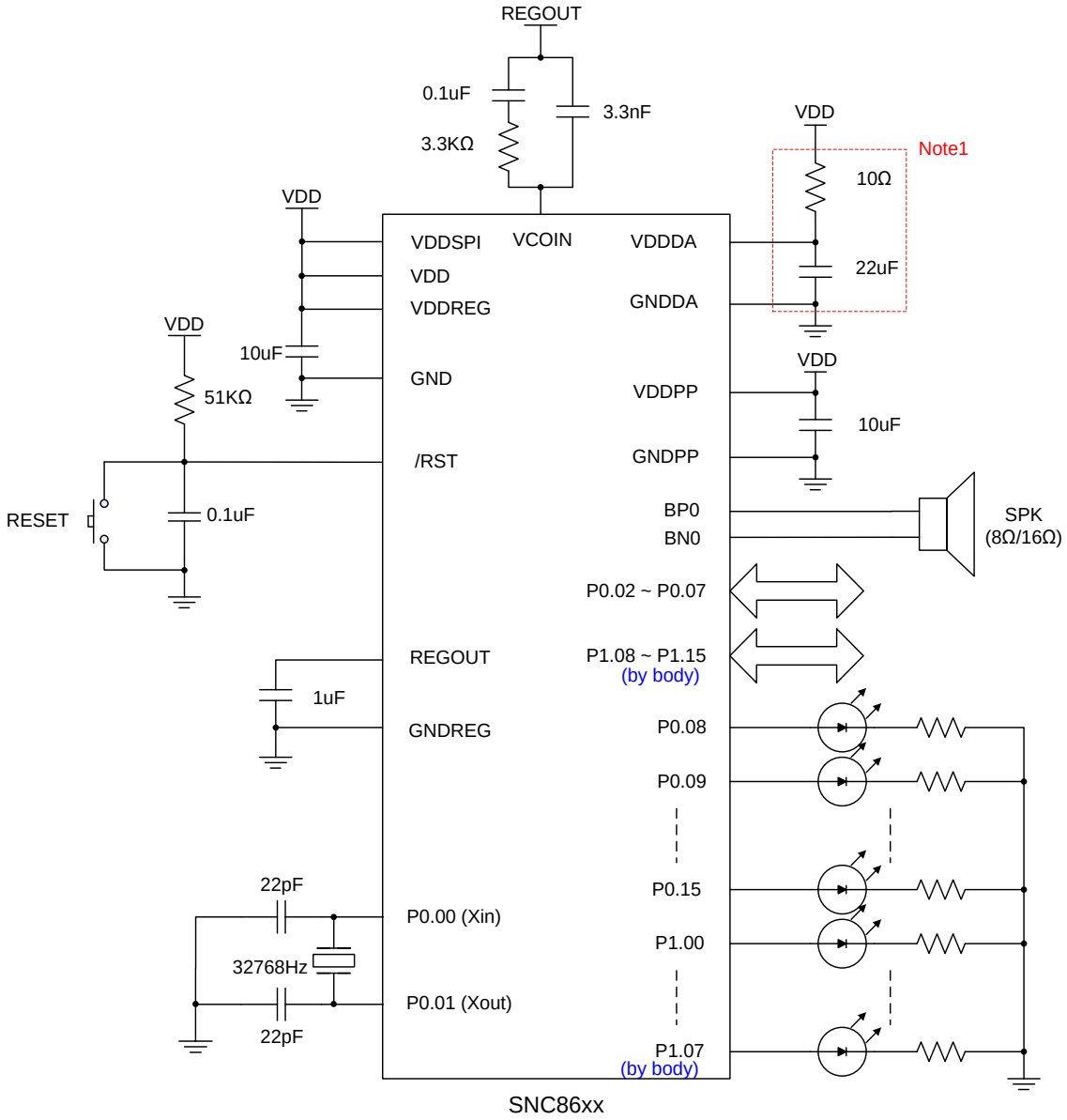


Note.

1. If system clock is selected PLL source, X'tal and PLL Low Pass Filter circuit must be connected.
2. REGOUT PIN is regulator output pin but also for CVDD input pin.
3. VDDSPI PIN must be connected to VDD, when no SPI application.

8.1.3 Application circuit with IO heavy loading

Power Supply: 2.2V ~ 5.5V

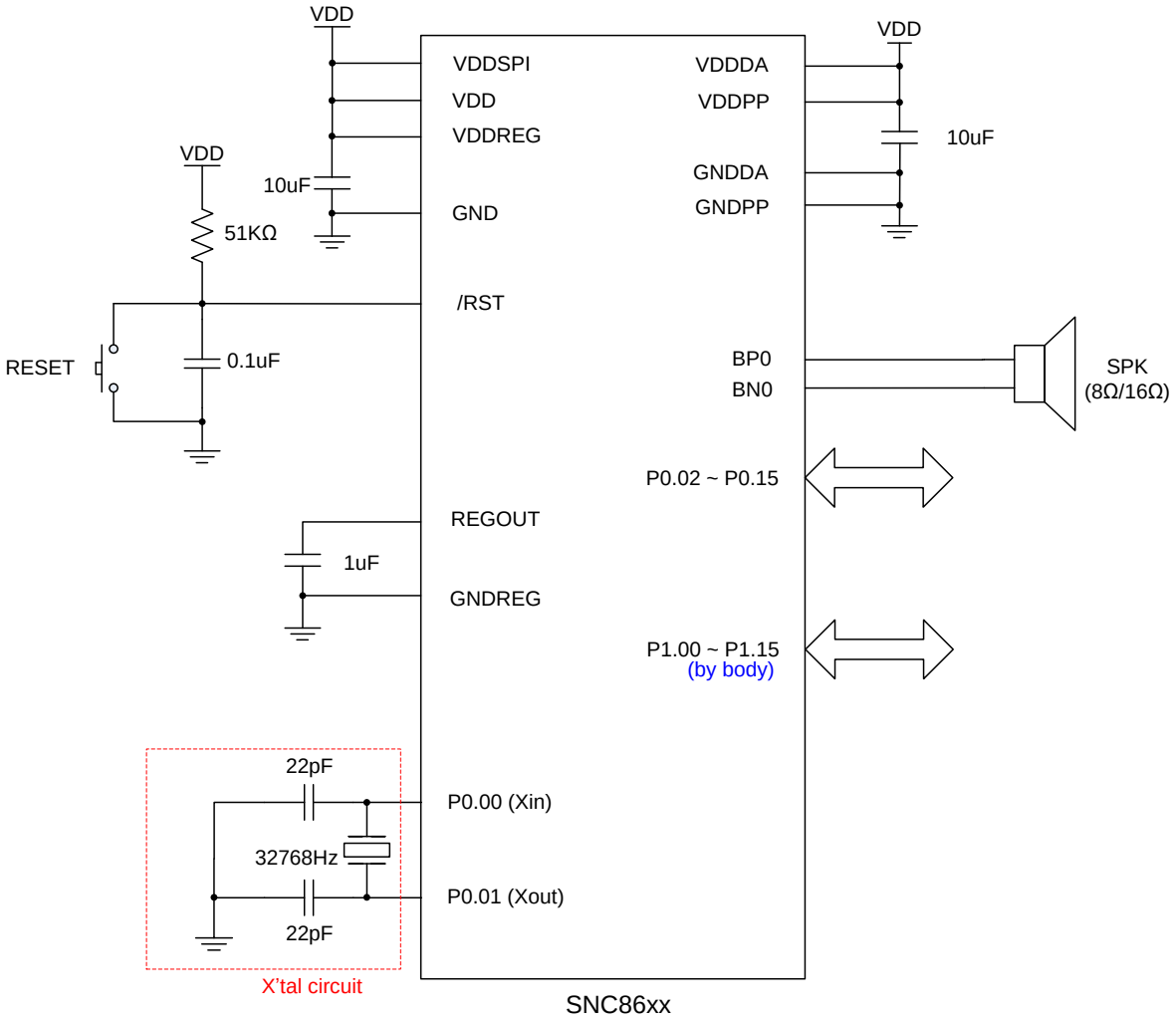


Note.

1. In high loading applications, considering system stability and performance, it is suggested to add a low-pass filter (10ohm and 22uF) on the DAC power group.
2. REGOUT PIN is regulator output pin but also for CVDD input pin.
3. VDDSPI PIN must be connected to VDD, when no SPI application.

8.1.4 Application circuit with Low Clock from External Crystal

Power Supply: 2.2V ~ 5.5V

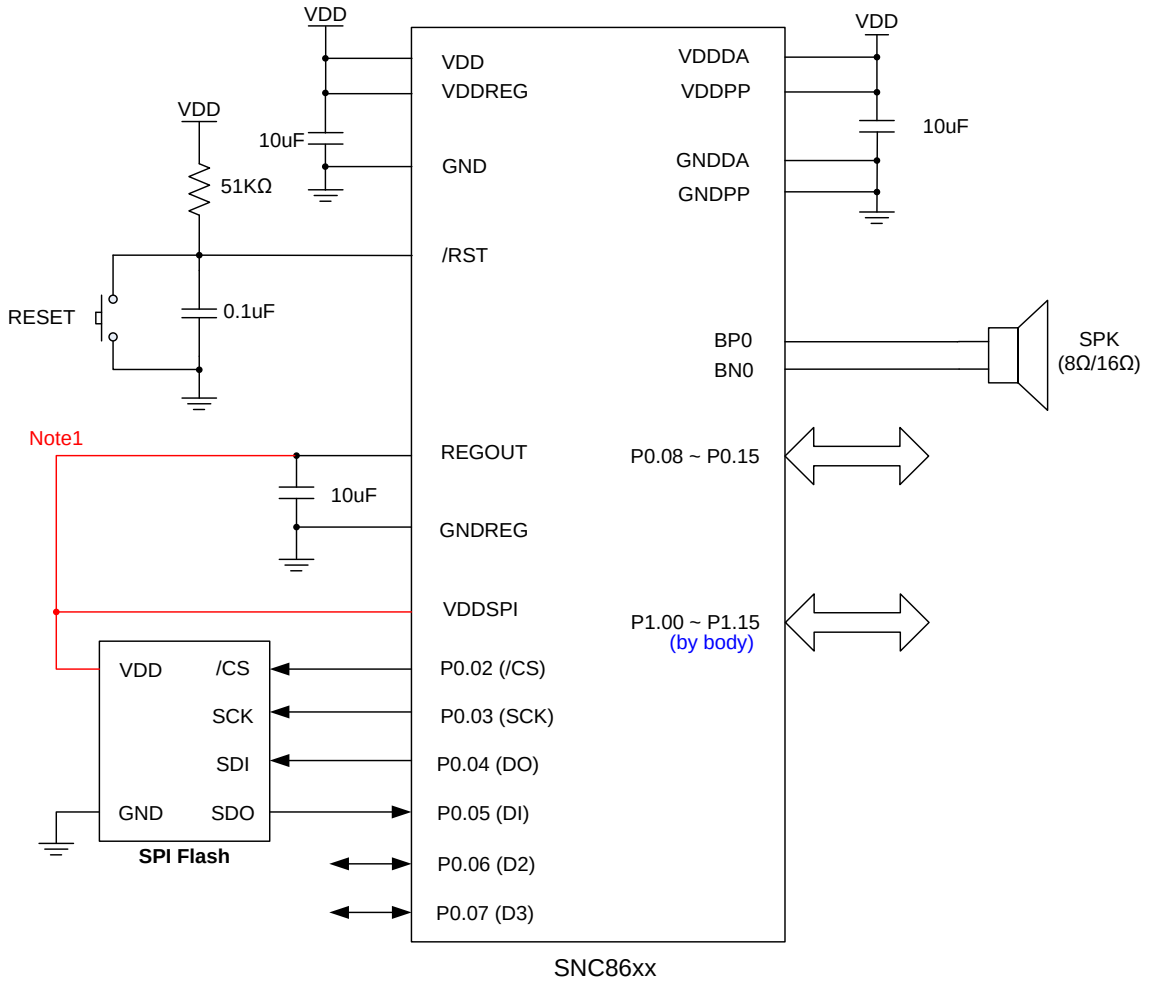


Note.

1. REGOUT PIN is regulator output pin but also for CVDD input pin.
2. VDDSPI PIN must be connected to VDD, when no SPI application.

8.1.5 Application circuit with SPI Flash

Power Supply: 2.2V ~ 5.5V

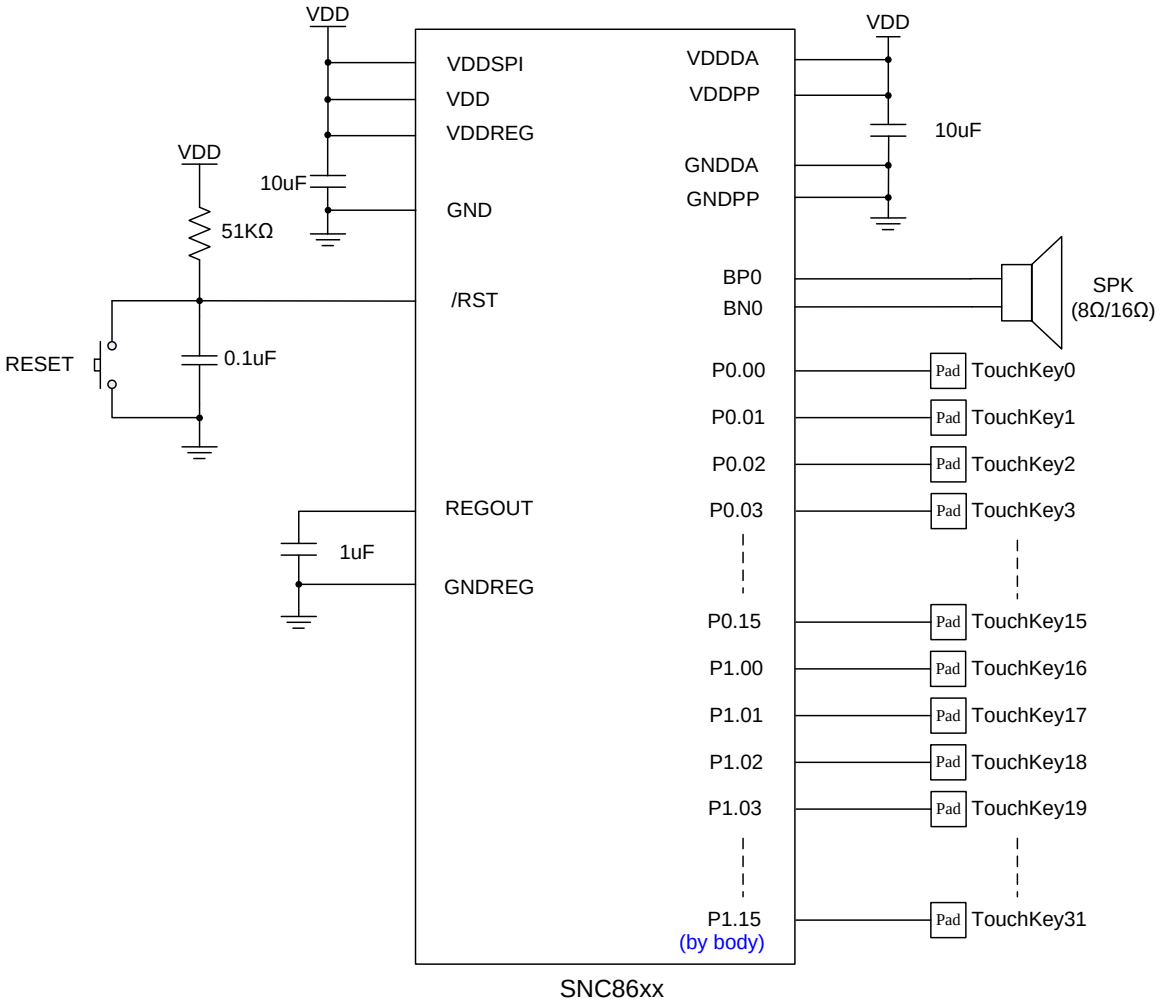


Note.

1. Note that the REGOUT pin must be connected to VDDSPI pin and SPI Flash power when system power is at 5V application. When VDDSPI pin connect to REGOUT pin the SPI interface (P0.02 ~ P0.07) power range is reference to REGOUT.
2. REGOUT PIN is regulator output pin but also for CVDD input pin.

8.1.6 Application circuit with Cap-Sensing

Power Supply: 2.2V ~ 5.5V



Note.

1. REGOUT PIN is regulator output pin but also for CVDD input pin.
2. VDDSPI PIN must be connected to VDD, when no SPI application.

9 ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{DD}	-0.3	6.0	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
Operating Temperature	T_a	0	60.0	°C
Storage Temperature	T_{STG}	-55.0	125.0	°C

10 ELECTRICAL CHARACTERISTICS

DC Characteristics (Ta = 25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.2	-	5.5	V	
Standby Current	I_{SBY}	-	-	3	uA	V_{DD}=3V
Operating Current1	I_{OP1}	-	4.0	-	mA	V_{DD}=3V, Push-Pull off, no load. Execute "NOP" instruction, Fcpu=6MHz (IHRC)
Operating Current2	I_{OP2}	-	5.0	-	mA	V_{DD}=3V, Push-Pull off, no load. Execute "NOP" instruction, Fcpu=6MHz (PLL)
Operating Current3	I_{OP3}	-	5.5	-	mA	V_{DD}=3V, Push-Pull on, no load. Execute "NOP" instruction, Fcpu=6MHz (IHRC)
IDLE Mode Current1	I_{IDLE1}	-	4.0	-	uA	V_{DD}=3V, CPU halt, Push-Pull off, 32K x'tal off, ILRC on
IDLE Mode Current2	I_{IDLE2}	-	6.0	-	uA	V_{DD}=3V, CPU halt, Push-Pull off, 32K x'tal on
Input Pull-high Resistance	R_{PH}	-	440K	-	Ω	V_{DD}=3V
Input Pull-low Resistance	R_{PL}	-	1M	-	Ω	V_{DD}=3V
Normal I/O Drive current (P0.00, P0.01, P1.08~P1.15)	I_{OH1}	-	6	-	mA	V_{DD}=3V, V_O=2.4V
Normal I/O Sink current (P0.00, P0.01, P1.08~P1.15)	I_{OL1}	-	8	-	mA	V_{DD}=3V, V_O=0.4V
High I/O Drive current (P0.08~P0.15, P1.00~P1.07)	I_{OH2}	-	8	-	mA	V_{DD}=3V, V_O=2.4V
High I/O Sink current (P0.08~P0.15, P1.00~P1.7)	I_{OL2}	-	14	-	mA	V_{DD}=3V, V_O=0.4V
SPI I/O Drive current (P0.02~P0.07)	I_{OH3}	-	12	-	mA	V_{DD}=3V, V_O=2.4V
SPI I/O Sink current (P0.02~P0.07)	I_{OL3}	-	12	-	mA	V_{DD}=3V, V_O=0.4V

Input Low voltage	V_{IL}	VSS	0.3*VDD	-	V	-
Input high voltage	V_{IH}	-	0.7*VDD	VDD	V	-
Low voltage Reset (LVR)	V_{RST}	-	2.0	-	V	-
System Clock (ROSC)	F_{SYS}		12.288		MHz	± 1.5% @3V
PPDAC drive current	I_{PPD}		300		mA	V_{DD}=3V, V_O=1.5V
PPDAC sink current	I_{PPS}		300		mA	V_{DD}=3V, V_O=1.5V

Regulator Characteristics (Ta=25 ^oC)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Voltage	V_{REGI}	2.2	4.5	5.5	V	
Output Voltage	V_{REGO}	2.8	3	3.2	V	Input Voltage = 4.5V
Maximum Current Output	I_{REGO}			35	mA	
Standby Current	I_{REGS}			1.5	uA	

11 Consumption of Playback in SPI Flash

Playback			SPI Flash Capacity(Unit: second)							
Algorithm	Sample Rate	Bit Rate (Kbps)	1Mbit	2Mbit	4Mbit	8Mbit	16Mbit	32Mbit	64Mbit	128Mbit
HQADPCM	8K	34.80	30.1	60.3	120.5	241.1	482.1	964.2	1928.4	3856.8
		43.04	24.4	48.7	97.5	194.9	389.8	779.6	1559.2	3118.4
	12K	52.20	20.1	40.2	80.4	160.7	321.4	642.8	1285.6	2571.2
		64.20	16.3	32.7	65.3	130.7	261.3	522.7	1045.3	2090.6
	16K	69.60	15.1	30.1	60.3	120.5	241.1	482.1	964.2	1928.4
		85.60	12.2	24.5	49.0	98.0	196.0	392.0	784.0	1568.0

12 Touch Application Current

Iidle : Idle current

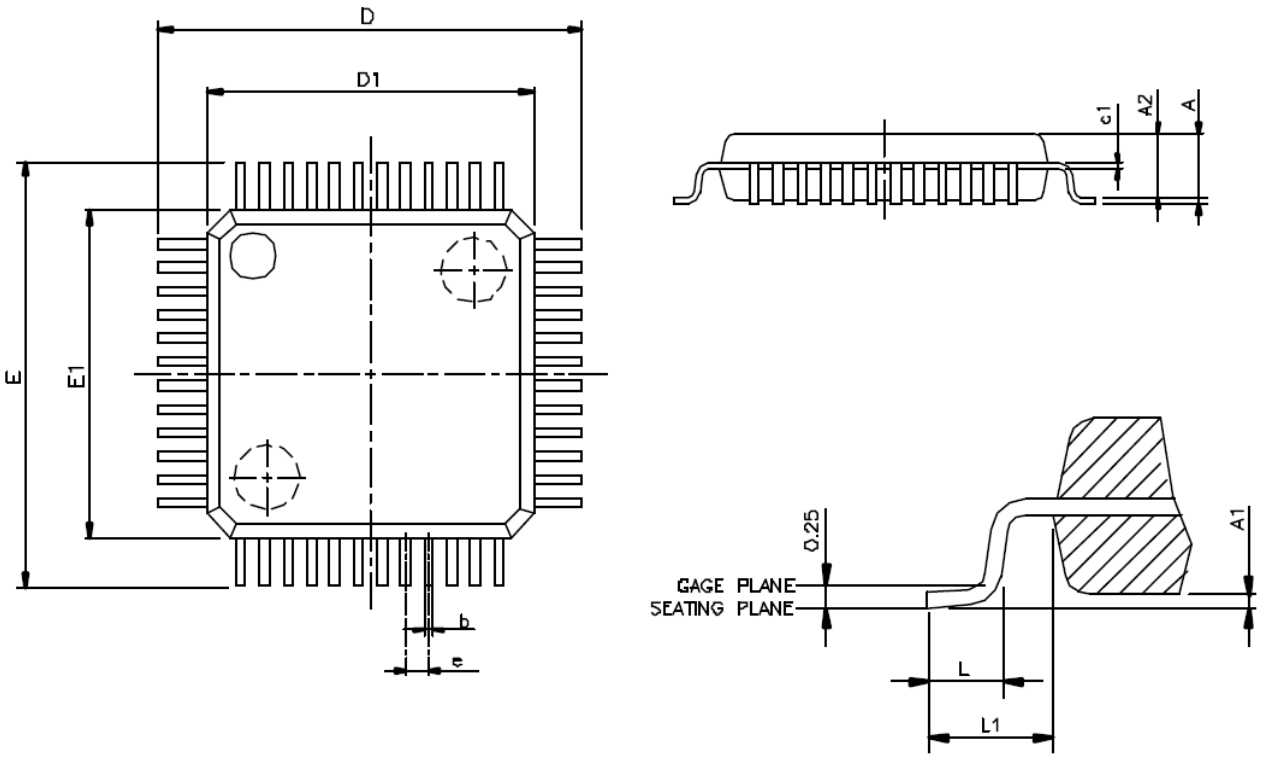
Iop : Operating current

Iidle=4uA Iop=5.8mA EachScanKeyTime=0.5ms			
Key Number	WakeUpTime	KeyScanTime	Current
	(s)	(ms)	(uA)
16CH	0.125	8.5	223.11
	0.250	8.5	113.56
	0.500	8.5	58.78
	1.000	8.5	31.39
8CH	0.125	4.5	120.00
	0.250	4.5	62.00
	0.500	4.5	33.00
	1.000	4.5	18.50
4CH	0.125	2.5	68.44
	0.250	2.5	36.22
	0.500	2.5	20.11
	1.000	2.5	12.06
2CH	0.125	1.5	42.67
	0.250	1.5	23.33
	0.500	1.5	13.67
	1.000	1.5	8.83
1CH	0.125	1.0	29.78
	0.250	1.0	16.89
	0.500	1.0	10.44
	1.000	1.0	7.22

Iidle=4uA Iop=5.8mA EachScanKeyTime=1.0ms			
Wake-up Key Number	Wake up Time (S)	KeyScanTime(ms)	Current
	(S)	(ms)	(uA)
16CH	0.125	17.0	442.22
	0.250	17.0	223.11
	0.500	17.0	113.56
	1.000	17.0	58.78
8CH	0.125	9.0	236.00
	0.250	9.0	120.00
	0.500	9.0	62.00
	1.000	9.0	33.00
4CH	0.125	5.0	132.89
	0.250	5.0	68.44
	0.500	5.0	36.22
	1.000	5.0	20.11
2CH	0.125	3.0	81.33
	0.250	3.0	42.67
	0.500	3.0	23.33
	1.000	3.0	13.67
1CH	0.125	2.0	55.56
	0.250	2.0	29.78
	0.500	2.0	16.89
	1.000	2.0	10.44

13 PACKAGE INFORMATION

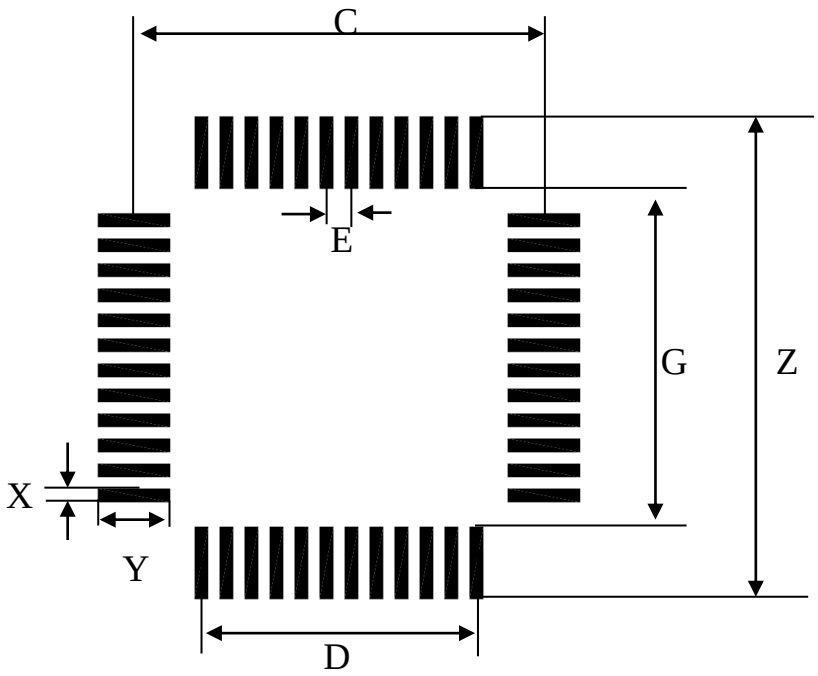
13.1. 48-pin LQFP (7x7x1.4mm)



Symbols	Min.	Max.
A	-	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
B	0.17	0.27
L	0.45	0.75
L1	1 REF	

UNIT: MM

SONiX LQFP48-7X7X1.4mm PCB Land Patten Dimensions Reference



Unit:mm

Package	Z	G	X	Y	C	D	E
				ref	ref	ref	ref
LQFP48-7X7	9.80	6.60	0.30	1.60	8.20	5.50	0.50

Note: Reference IPC-SM-782 Standard

14 DISCLAIMER

The information appearing in SONiX web pages (“this publication”) is believed to be accurate. However, this publication could contain technical inaccuracies or typographical errors.

The reader should not assume that this publication is error-free or that it will be suitable for any particular purpose. SONiX makes no warranty, express, statutory implied or by description in this publication or other documents which are referenced by or linked to this publication. In no event shall SONiX be liable for any special, incidental, indirect or consequential damages of any kind, or any damages whatsoever, including, without limitation, those resulting from loss of use, data or profits, whether or not advised of the possibility of damage, and on any theory of liability, arising out of or in connection with the use or performance of this publication or other documents which are referenced by or linked to this publication.

This publication was developed for products offered in Taiwan. SONiX may not offer the products discussed in this document in other countries. Information is subject to change without notice. Please contact SONiX or its local representative for information on offerings available. Integrated circuits sold by SONiX are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only.

The application circuits illustrated in this document are for reference purposes only. SONIX DISCLAIMS ALL WARRANTIES, INCLUDING THE WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. SONIX reserves the right to halt production or alter the specifications and prices, and discontinue marketing the Products listed at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders.

Products described herein are intended for use in normal commercial applications.

Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by SONIX for such application.